

BANDON/NorthBay 13" Schematics Document


Whiskey Lake -U 42

2019-02-12

REV:A00

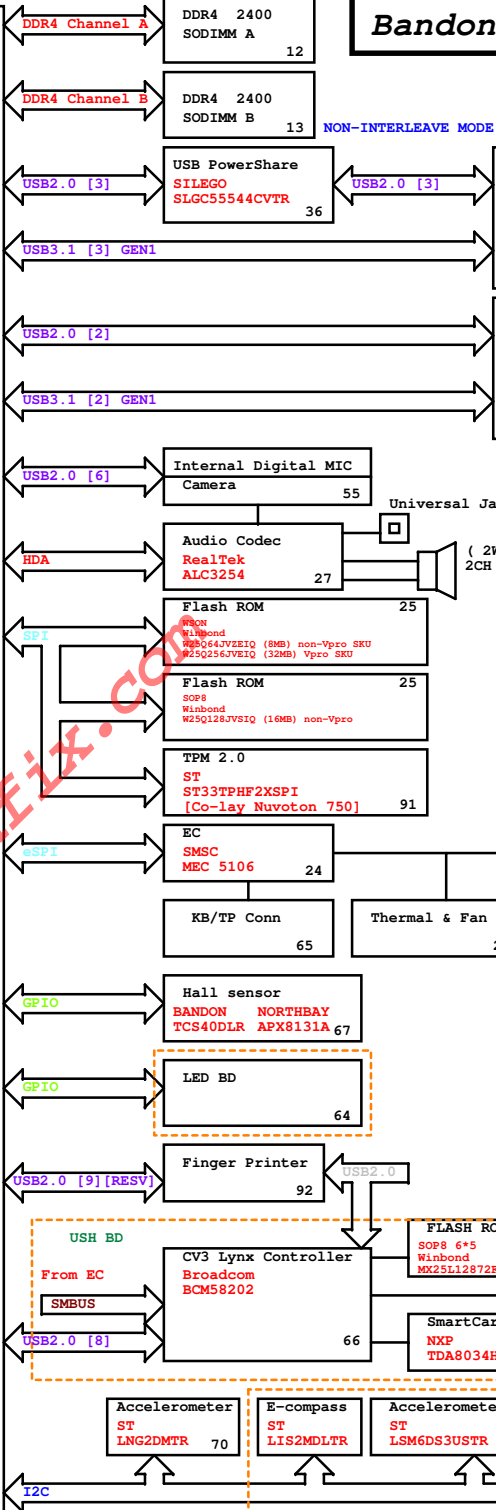
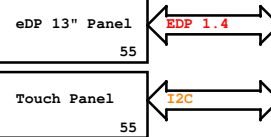
DY : None Installed  
WWAN:For WWAN installed  
LAN:For LAN Installed  
Sensor:For Sensor Installed  
Debug:For Debug Port installed

<Core Design>

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Title <b>Cover Page</b>			
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Project code : 4PD0G3010001  
PCB P/N : 18717  
Revision : -1

Lat Function	R45/Transformer	Bandon	NorthBay
	De-pop	Pop	De-pop
	De-pop	Pop	De-pop
Sensor Board	De-pop	Pop	De-pop
	De-pop	Pop	De-pop
	De-pop	Pop	De-pop
	De-pop	Pop	De-pop
Lead Board	De-pop	Pop	De-pop
	De-pop	Pop	De-pop



## Bandon/Northbay 13" Block Diagram

Charger		44
ISL9538HRTZ-GP-U		
INPUTS	OUTPUTS	
BT+	DCBATOUT	
SYSTEM DC/DC		45
SY8288BRAC/SY8288CRAC		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5	
	3D3V_S5	
	5V_AUX_S5	
	5V_S5	
CPU DC/DC		47
FDMF3035-GP		
INPUTS	OUTPUTS	
DCBATOUT	1V_VCCGT	
CPU DC/DC		50
ISL95808HRZ-T-1-GP		
INPUTS	OUTPUTS	
DCBATOUT	1V_VCCSA	
SYSTEM DC/DC		51
SY8288RAC		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3	
SYSTEM DC/DC		52
AOZ2260QI-10-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S5	
SYSTEM DC/DC		54
RT6542AGQW-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_VCCPRIM_CORE	
Load Switches		
INPUTS	OUTPUTS	
3D3V_S5	3D3V_S5_PCH	
	3D3V_LAN	
	3D3V_S5_WWAN	
	3D3V_S5_WLAN	
	2D5V_S3	
	1D8V_S5	
	VCDVDD_FUSE	
	3D3V_S0	
3D3V_S0	+3V_AVDD	
	3D3V_CAMERA_S0	
	3D3V_S0_SATA	
5V_S5	5V_S0	
	1D05V_VCCIO	
5V_S0	+5V_PVDD	
	5V_TSP_S0	
	5V_HDMI	
1D8V_S5	1D8V_S0	
1D2V_S3	0D6V_S0	
	1D2V_VCCPLL_OC	
1D05V_S5	1D05V_VCCSTG	
	1D05V_VCCSTG	
PCB LAYER (FR4-10 Layer)		
L1: Top	L6: Signal	
L2: GND	L7: GND/PWR	
L3: Signal	L8: Signal	
L4: GND	L9: GND	
L5: Signal	L10: Bottom	

# Main Func = CPU

[24]	PECI_CPU	<< >>
[24,43,44,46]	PROCHOT#_CPU	<< >>
[24]	THERMTRIP#_CPU	<< >>
[99]	BPM_N0	<<< >>>
[99]	BPM_N1	<<< >>>
[99]	CPU_JTAG_TCK	<< >>
[99]	CPU_JTAG_TDI	<< >>
[99]	CPU_JTAG_TDO	<< >>
[99]	CPU_JTAG_TMS	<< >>
[99]	CPU_JTAG_TRST#	<< >>
[99]	CPU_JTAG_PRDY#	<< >>
[99]	CPU_JTAG_PREQ#	<< >>
[99]	PCH_JTAG_TCK	<< >>
[17]	H_CUPWRGD	>> >>
[55]	TOUCH_SCREEN_PD#_R	>> >>
[24,65]	TOUCHPAD_INTR#	>> >>
[55]	TOUCH_SCREEN_DET#	>> >>

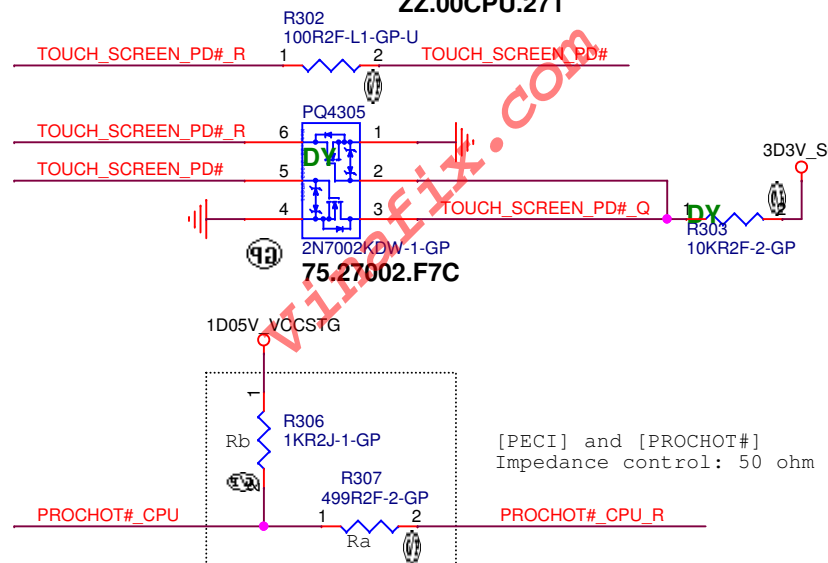
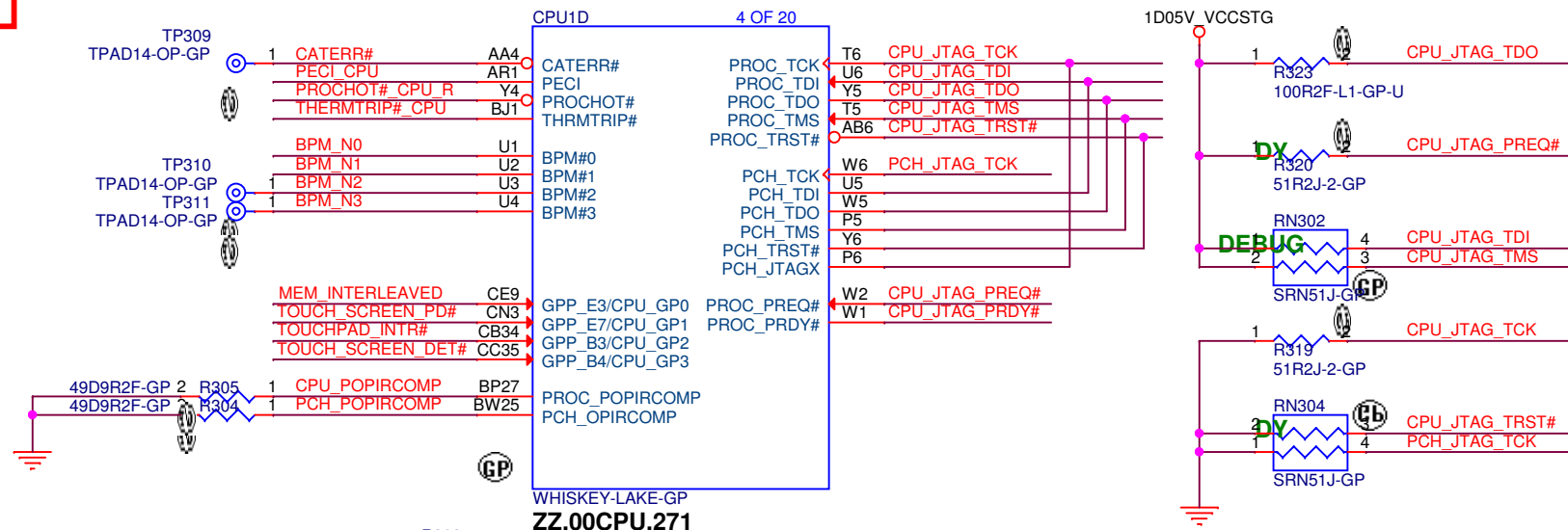
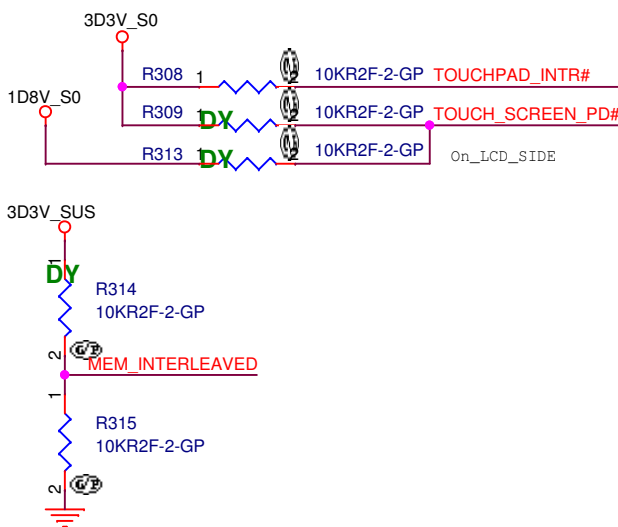
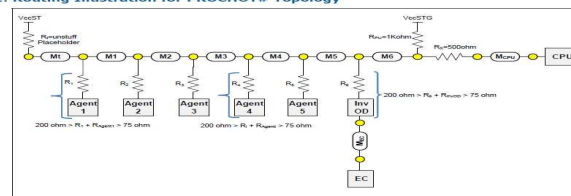


Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches  
M6: 1-11 inches  
MCPU: 0.3-1.5 inches  
Mt <0.3 mils  
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

DIMM_TYPE	
LOW	HIGH
NON_INTERLEAVED	INTERLEAVED

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# Main Func = CPU

## Edp

[55] eDP\_TX\_CPU\_N0 <<<  
[55] eDP\_TX\_CPU\_P0 <<<  
[55] eDP\_TX\_CPU\_N1 <<<  
[55] eDP\_TX\_CPU\_P1 <<<

[55] eDP\_AUX\_CPU\_N <<<  
[55] eDP\_AUX\_CPU\_P <<<

[55] EDP\_HPD >>>

[55] eDP\_BLEN\_CPU <<<  
[55] eDP\_BLCTRL\_CPU <<<  
[55] eDP\_VDDEN\_CPU <<<

## DP to HDMI

[57] HDMI\_DDI\_TX\_N2 <<<  
[57] HDMI\_DDI\_TX\_P2 <<<  
[57] HDMI\_DDI\_TX\_N1 <<<  
[57] HDMI\_DDI\_TX\_P1 <<<  
[57] HDMI\_DDI\_TX\_N0 <<<  
[57] HDMI\_DDI\_TX\_P0 <<<  
[57] HDMI\_DDI\_TX\_N3 <<<  
[57] HDMI\_DDI\_TX\_P3 <<<

[57] HDMI\_DET\_CPU >>>

[57] HDMI\_SCL\_CPU <<<  
[57] HDMI\_SDA\_CPU <<<

## DP to AR

[71] DP2\_DDI\_TX\_N0 <<<  
[71] DP2\_DDI\_TX\_P0 <<<  
[71] DP2\_DDI\_TX\_N1 <<<  
[71] DP2\_DDI\_TX\_P1 <<<  
[71] DP2\_DDI\_TX\_N2 <<<  
[71] DP2\_DDI\_TX\_P2 <<<  
[71] DP2\_DDI\_TX\_N3 <<<  
[71] DP2\_DDI\_TX\_P3 <<<

[71] DP2\_AUX\_CPU\_P <<<  
[71] DP2\_AUX\_CPU\_N <<<

[71,72] DP2\_HPD\_CPU <<<

## DP to HDMI

HDMI\_DDI\_TX\_N2 AL5  
HDMI\_DDI\_TX\_P2 AL6  
HDMI\_DDI\_TX\_N1 AJ5  
HDMI\_DDI\_TX\_P1 AJ6  
HDMI\_DDI\_TX\_N0 AF6  
HDMI\_DDI\_TX\_P0 AF5  
HDMI\_DDI\_TX\_N3 AE5  
HDMI\_DDI\_TX\_P3 AE6

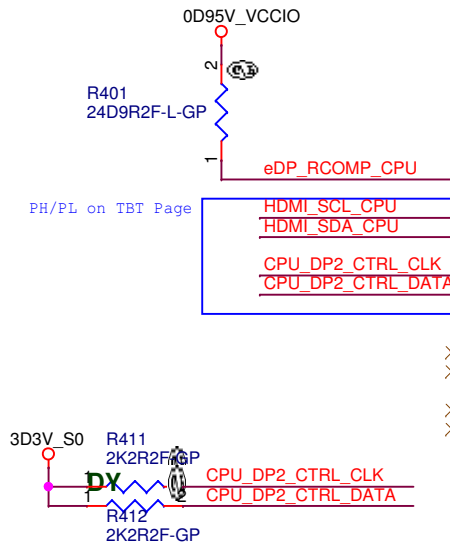
## DP to MUX

DP2\_DDI\_TX\_N0 AC4  
DP2\_DDI\_TX\_P0 AC3  
DP2\_DDI\_TX\_N1 AC1  
DP2\_DDI\_TX\_P1 AC2  
DP2\_DDI\_TX\_N2 AE4  
DP2\_DDI\_TX\_P2 AE3  
DP2\_DDI\_TX\_N3 AE1  
DP2\_DDI\_TX\_P3 AE2

## 575412 eDP\_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 or 100 $\Omega$ $\pm$ 1%	600 mils

Note: Must maintain low DC resistance routing (<0.1 $\Omega$ )



		CPU (TBT, DP1.4, USB3.1 g2)				
		eDP DDI A	DDI 1	DDI 2		
North Bay 13 Bandon	13 UU (non-TBT)	LCD	HDMI 1.4		Type-C Port 1	
	13 UU (TBT)	LCD	TBT (Alpine Ridge Port 0)		TBT (Alpine Ridge Port 1)	HDMI on AR side-port

## CPU1A

DDI1\_TXN0  
DDI1\_TXP0  
DDI1\_TXN1  
DDI1\_TXP1  
DDI1\_TXN2  
DDI1\_TXP2  
DDI1\_TXN3  
DDI1\_TXP3

DDI2\_TXN0  
DDI2\_TXP0  
DDI2\_TXN1  
DDI2\_TXP1  
DDI2\_TXN2  
DDI2\_TXP2  
DDI2\_TXN3  
DDI2\_TXP3

DDI1\_AUX\_N  
DDI1\_AUX\_P  
DDI2\_AUX\_N  
DDI2\_AUX\_P  
DDI3\_AUX\_N  
DDI3\_AUX\_P

DISP\_UTILS  
DISP\_RCOMP  
GPP\_E13/DDPB\_HPD0/DISP\_MISC0  
GPP\_E14/DDPC\_HPD1/DISP\_MISC1  
GPP\_E15/DPPD\_HPD2/DISP\_MISC2  
GPP\_E16/DPPD\_HPD3/DISP\_MISC3  
GPP\_E17/EDP\_HPD/DISP\_MISC4

EDP\_BKLTEN  
EDP\_VDDEN  
EDP\_BKLTCTL  
GPP\_E18/DDPB\_CTRLCLK/CNV\_BT\_HOST\_WAKE#  
GPP\_E19/DDPB\_CTRLCLK  
GPP\_E20/DPPC\_CTRLCLK  
GPP\_E21/DPPC\_CTRLCLK  
GPP\_E22/DPPD\_CTRLCLK  
GPP\_E23/DPPD\_CTRLCLK  
GPP\_H16/DDPF\_CTRLCLK  
GPP\_H17/DDPF\_CTRLCLK

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EDP\_TXN0  
EDP\_TXP0  
EDP\_TXN1  
EDP\_TXP1  
EDP\_TXN2  
EDP\_TXP2  
EDP\_TXN3  
EDP\_TXP3

EDP\_AUX\_N  
EDP\_AUX\_P  
DISP\_UTILS  
DDI1\_AUX\_N  
DDI1\_AUX\_P  
DDI2\_AUX\_N  
DDI2\_AUX\_P  
DDI3\_AUX\_N  
DDI3\_AUX\_P

GPP\_E13/DDPB\_HPD0/DISP\_MISC0  
GPP\_E14/DDPC\_HPD1/DISP\_MISC1  
GPP\_E15/DPPD\_HPD2/DISP\_MISC2  
GPP\_E16/DPPD\_HPD3/DISP\_MISC3  
GPP\_E17/EDP\_HPD/DISP\_MISC4

EDP\_BKLTEN  
EDP\_VDDEN  
EDP\_BKLTCTL  
GPP\_E18/DDPB\_CTRLCLK/CNV\_BT\_HOST\_WAKE#  
GPP\_E19/DDPB\_CTRLCLK  
GPP\_E20/DPPC\_CTRLCLK  
GPP\_E21/DPPC\_CTRLCLK  
GPP\_E22/DPPD\_CTRLCLK  
GPP\_E23/DPPD\_CTRLCLK  
GPP\_H16/DDPF\_CTRLCLK  
GPP\_H17/DDPF\_CTRLCLK

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AG4 eDP\_TX\_CPU\_N0  
AG3 eDP\_TX\_CPU\_P0  
AG2 eDP\_TX\_CPU\_N1  
AG1 eDP\_TX\_CPU\_P1  
AJ4  
AJ3  
AJ2  
AJ1

AH4 eDP\_AUX\_CPU\_N  
AH3 eDP\_AUX\_CPU\_P  
AM7  
AC7  
AC6  
AD4  
AD3  
AG7  
AG6

CN6 HDMI\_DET\_CPU\_R  
CM6 DP2\_HPD\_CPU\_R  
CP7  
CP6 FFS\_INT2  
CM7 EDP\_HPD  
CK11 eDP\_BLEN\_CPU  
CG11 eDP\_VDDEN\_CPU  
CH11 eDP\_BLCTRL\_CPU

3D3V\_S5\_PCH  
R405 10KR2J-3-GP  
R406 10KR2J-3-GP  
HDMI\_DET\_CPU\_R  
HDMI\_DET\_CPU  
HDMI\_DET\_CPU\_P  
2N7002KDW-1-GP  
75.27002.F7C  
R403 100KR2J-1-GP

3D3V\_S5\_PCH  
R407 10KR2J-3-GP  
R408 10KR2J-3-GP  
DP2\_HPD\_CPU\_R  
DP2\_HPD\_CPU  
CPU\_DP2\_HPD\_P  
2N7002KDW-1-GP  
75.27002.F7C  
R410 100KR2J-1-GP

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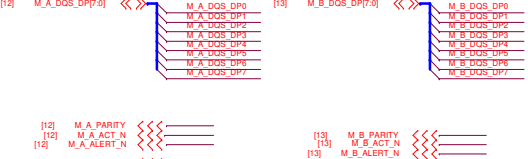
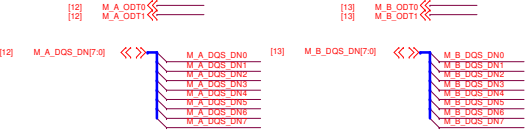
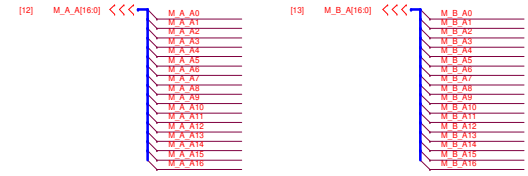
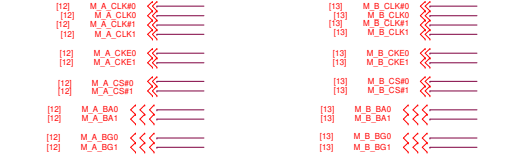
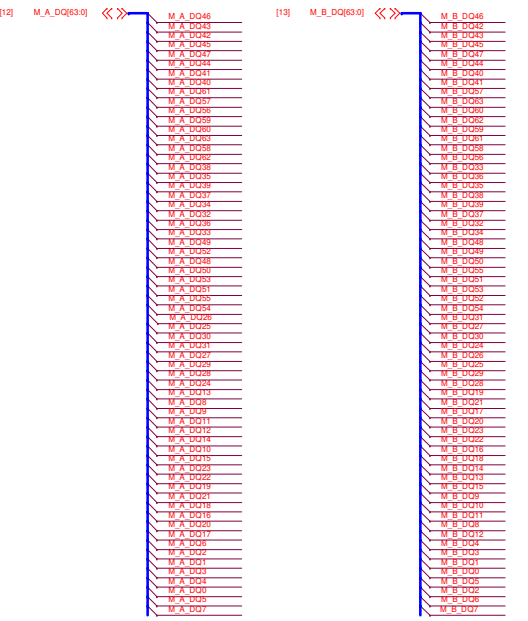
Title CPU\_(JTAG/CPU SIDE BAND)

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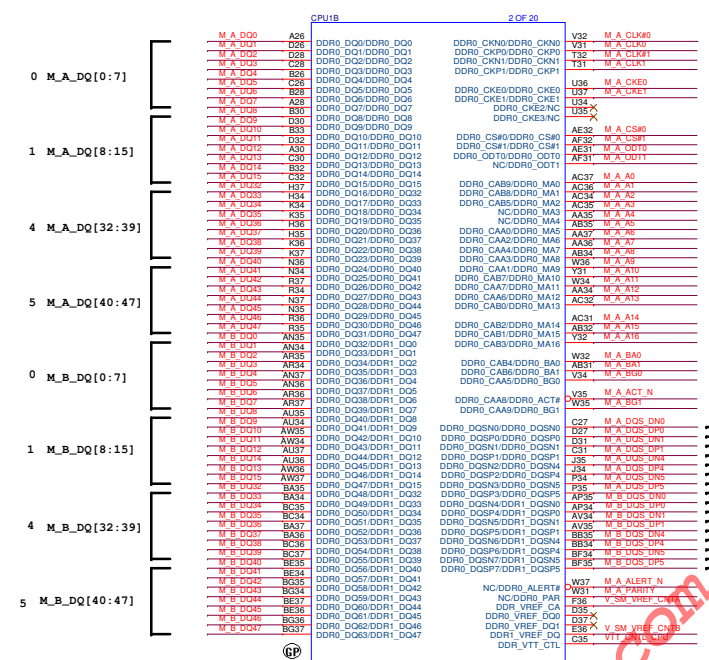
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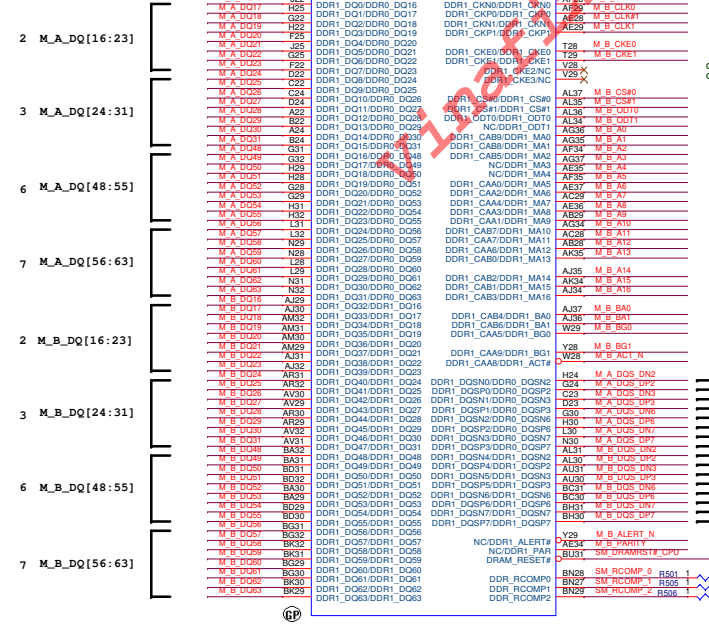
Main Func = CPU



DDR4 ball type: NON- Interleaved Type



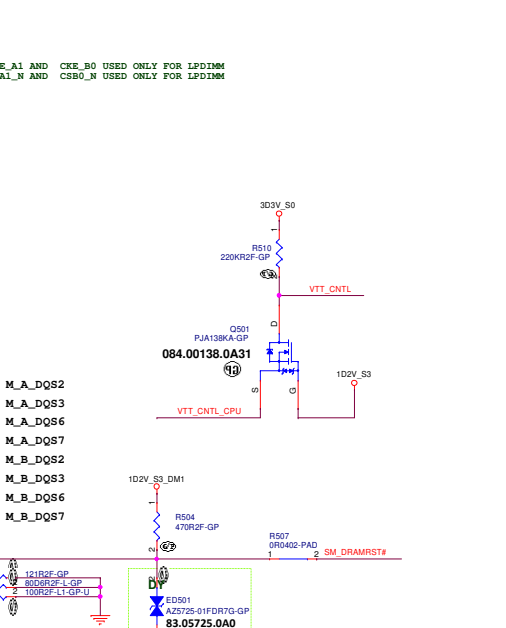
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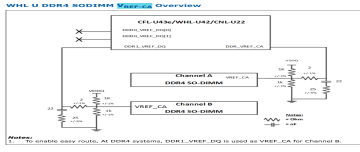
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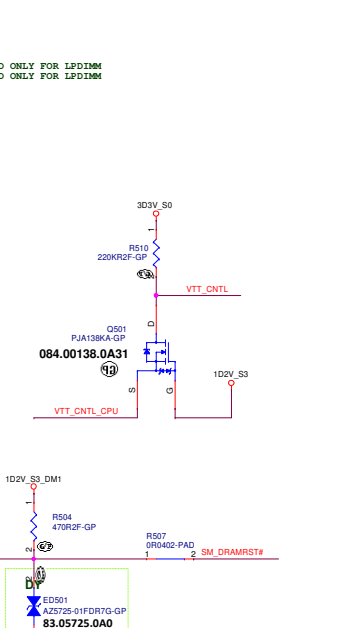
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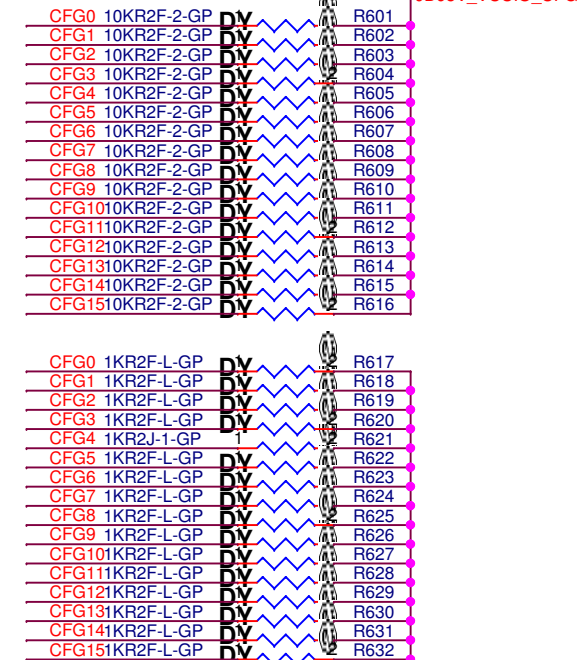
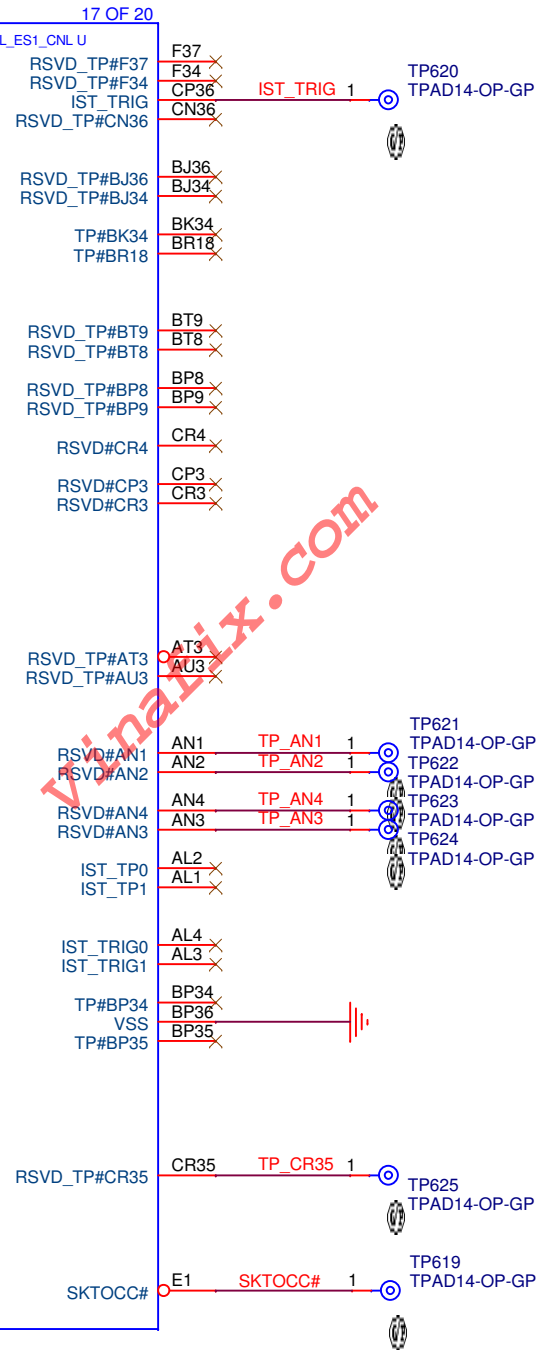
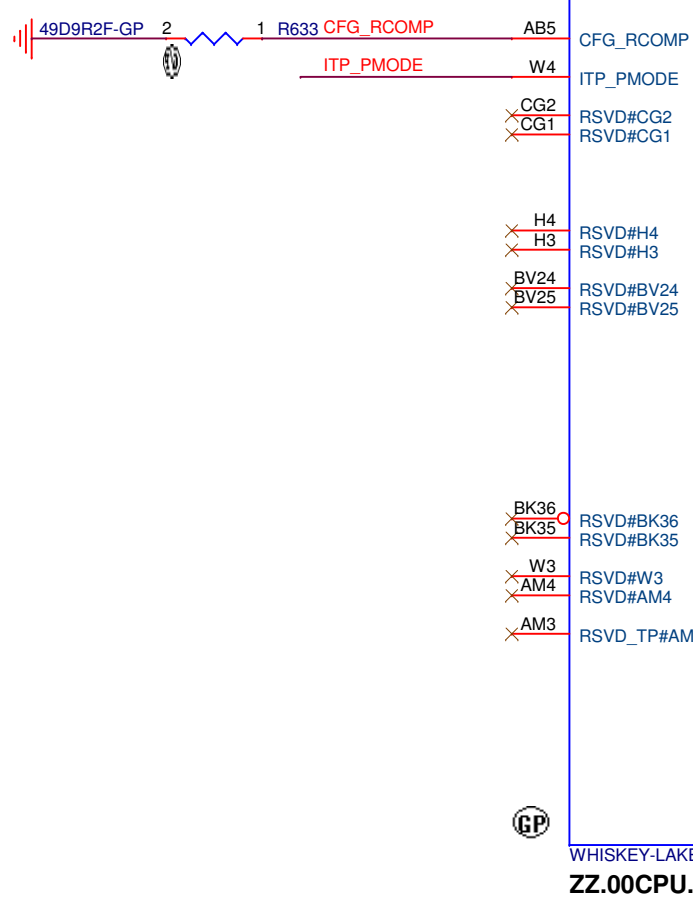
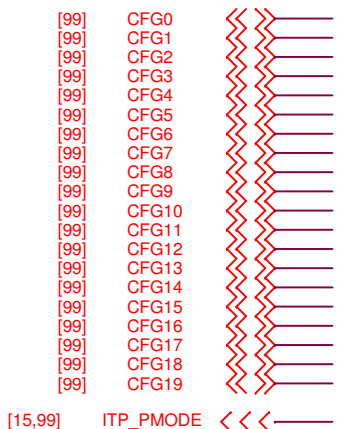


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5 | **Main Func = CPU**



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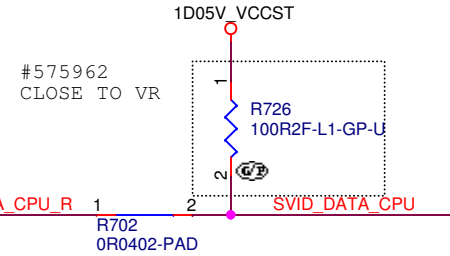
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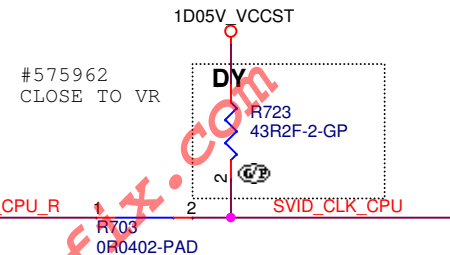
Layout Note:

The total Length of Data and Clock (from CPU to each VR) must be equal ( $\pm 0.1$  inch).  
Route the Alert signal between the Clock and the Data signals.

## SVID DATA



## SVID CLOCK



## SVID ALERT

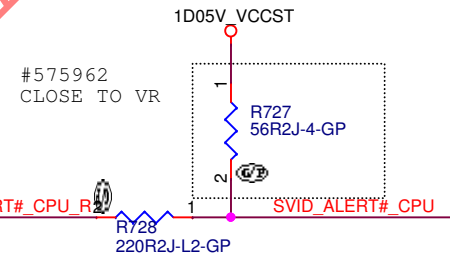
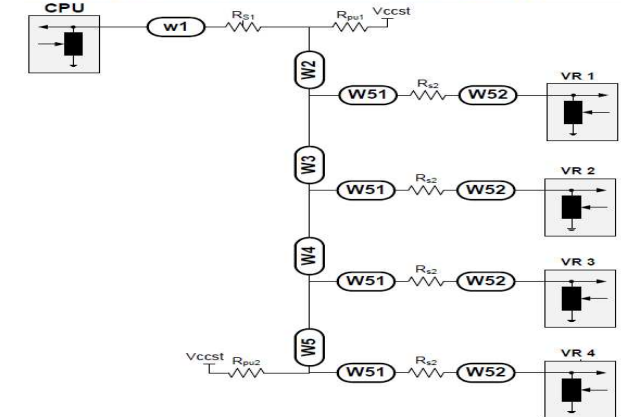


Table 10-10.SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>bus</sub> [Ω]	R <sub>bus</sub> [Ω]	R <sub>bus</sub> [Ω]	R <sub>bus</sub> [Ω]	W <sub>CPU</sub> [inches]
VIDSOUT											
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	
VIDALERT#							Empty	45	0	50	1.0

Figure 10-7. Routing Illustration for SVID Topology



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**CPU(VCC CORE)**

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A4

Document Number

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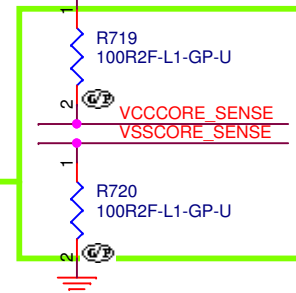
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**Layout Note:**

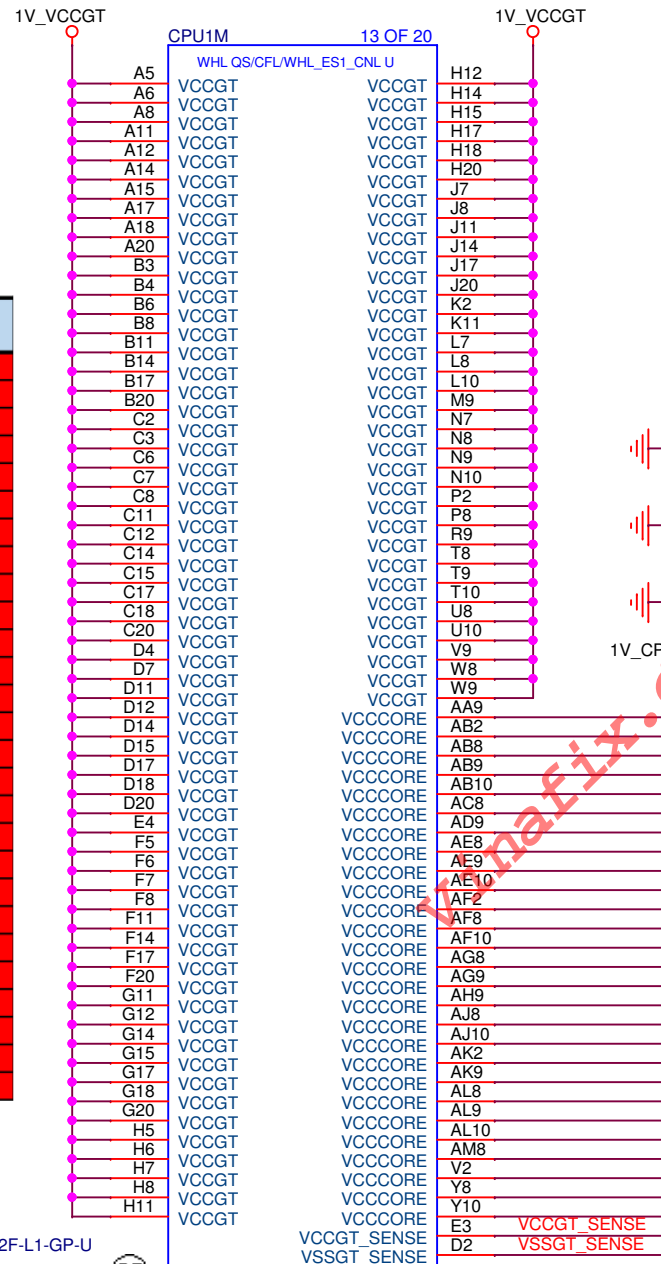
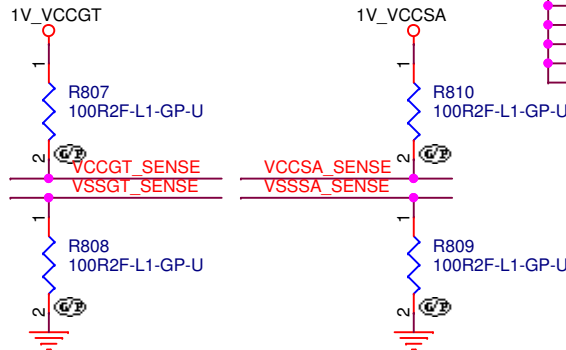
1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Length match<25mil



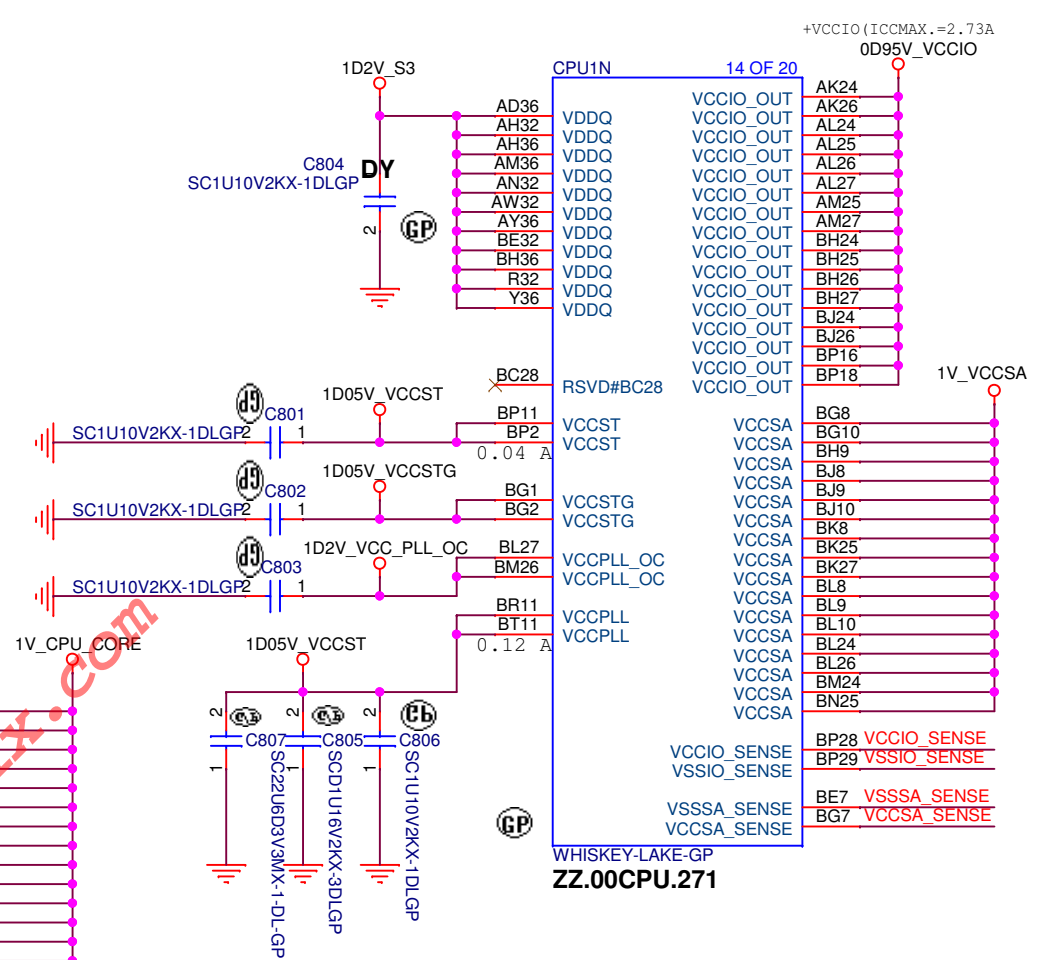
# Main Func = CPU

[46] VCCGT\_SENSE <<<< —  
[46] VSSGT\_SENSE <<<< —  
[46] VSSA\_SENSE <<<< —  
[46] VCSSA\_SENSE <<<< —  
[54] VCCIO\_SENSE >>>> —  
[54] VSSIO\_SENSE >>>> —

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



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VCCPLL_OC	1x 1uF 0402		Do not merge VccPLL, VccPLL_OC and VccST to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VccPLL	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		Placeholder Only. Can be placed on as either Primary or back side cap.
VccST	1x 1uF 0402		
VccSTG	1x 1uF 0402		

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Title

**CPU (DISPLAY)**

Size  
A4

Document Number

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 9 of	106

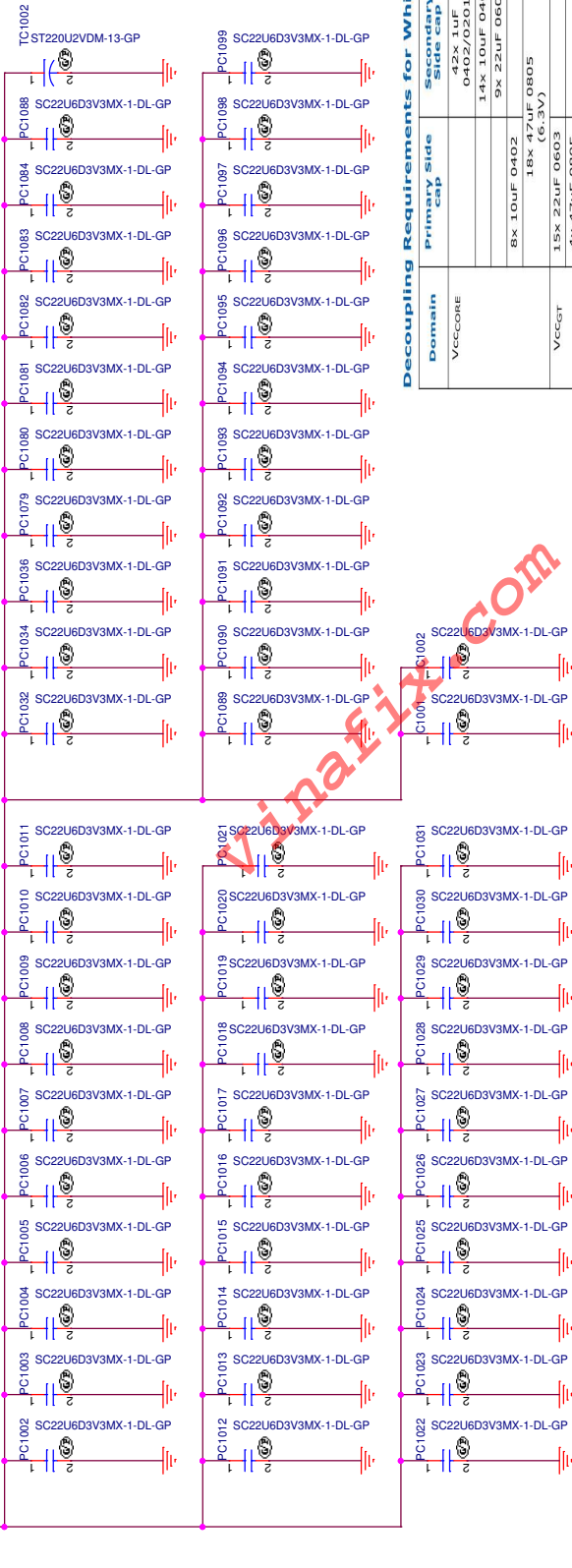


Main Func = CPU

Follow RO13 CAP account and vaule .

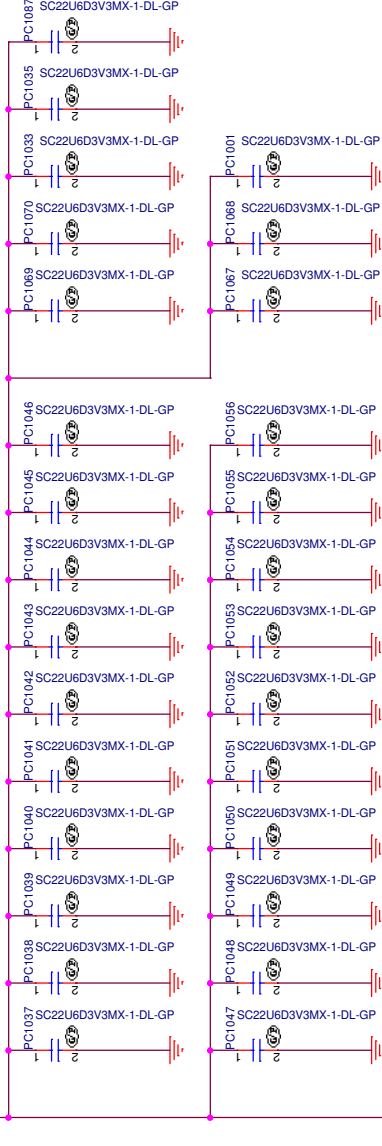
1V\_CPU\_CORE

220\*52/2200\*1  
1V\_CPU\_CORE



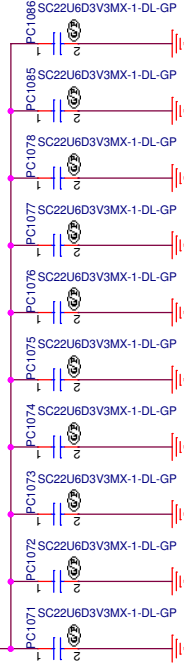
1V\_VCCGT

220 x 38  
1V\_VCCGT



1V\_VCCSA

220 x 10  
1V\_VCCSA



Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
	8x 10uF 0402	9x 22uF 0603	
	18x 47uF 0805 (6.3V)		Place as close to the package as possible
VCCGT	15x 22uF 0603 (6.3V)		Place as close to the package as possible.
	4x 47uF 0805 (6.3V)		Can be placed on as either Primary or back side cap.
			Place as close to the package as possible
		11x 1uF 0402/0201	
		15x 10uF 0402	Place as close to the package as possible

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCSA		4x 0402	Placeholder only.
	6x 10uF 0402	7x 10uF 0402	
	2x 47uF 0805 (6.3V)		
	2x 0805		Placeholder Only

Whiskey Lake U 4+2/Whiskey Lake U 4+2+/Cannon Lake U 2+2/ Coffee Lake U 4+3e Bulk Decoupling Example

Bulk Decoupling Location	Example WHL U42	Example WHL U42F	Example CFL U43e	Notes
VCCORE Power VR Primary side output	4x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	TBD	Placed at primary side output near to VR
VCCSA Power VR Primary side output	4x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	TBD	Placed at primary side output near to VR
VCCGT Power VR Primary side output	4x 220uF (@4.5mV ESR)	3x 220uF (@4.5mV ESR)	4x 220uF (@4.5mV ESR)	Placed at primary side output near to VR

**Notes:**

- These examples are based on 1414Hz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR. Bulk decoupling is not a requirement for all designs. Please consult your VR vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

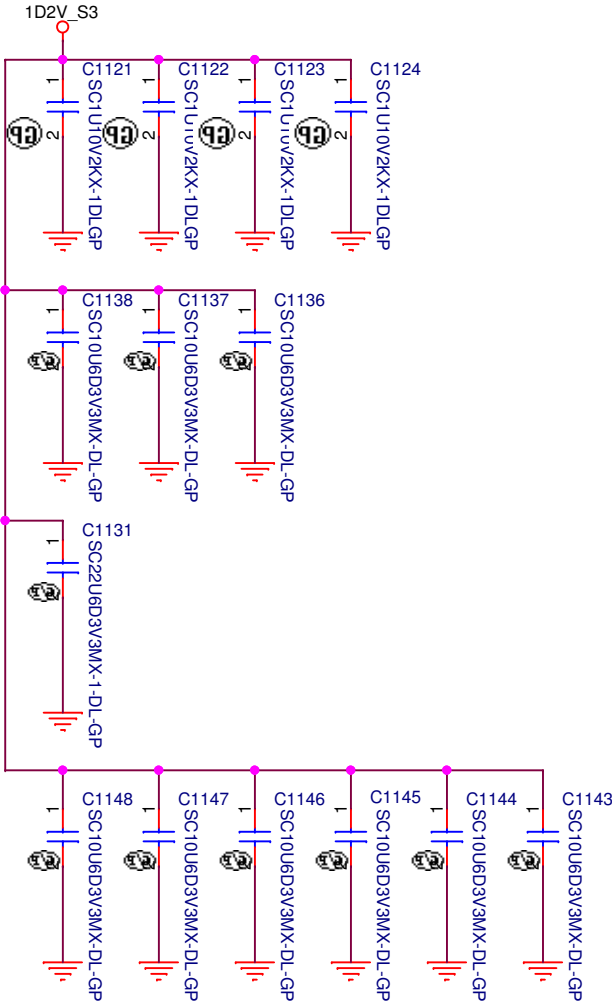
**DELL** Wistron Corporation  
21F, 88 Sec 1, Hsin Tai Rd., Hsinchu, Taiwan, R.O.C.

CPU (Power CAP1)

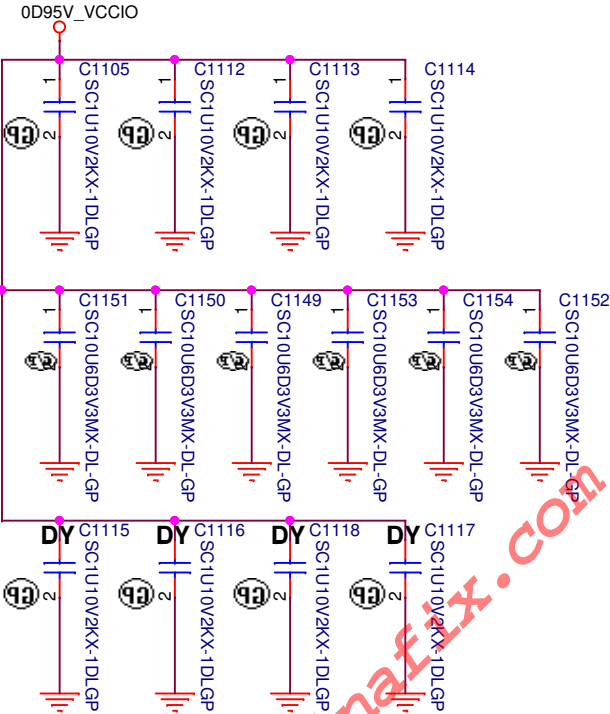
Size A3 Document Number Bandon / NorthBay 13" Rev x00  
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Main Func = CPU

VDDQ




VCCIO



V <sub>DDQ</sub>		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
V <sub>CCIO</sub>	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		Placeholder Only

<Core Design>



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Title

**CPU (Power CAP2)**

Size  
A4

Document Number  
**Bandon / NorthBay 13"**

Rev  
**X00**

Date: Friday, February 15, 2019

Sheet 11 of 106



```

[0] M_A_A16[0] >>> M_A_A0
[M] M_A_A1
[M] M_A_A2
[M] M_A_A3
[M] M_A_A4
[M] M_A_A5
[M] M_A_A6
[M] M_A_A7
[M] M_A_A8
[M] M_A_A9
[M] M_A_A10
[M] M_A_A11
[M] M_A_A12
[M] M_A_A13
[M] M_A_A14
[M] M_A_A15
[M] M_A_A16

[5] M_A_BA0 >>>
[5] M_A_BA1 >>>
[5] M_A_B00 >>>
[5] M_A_B01 >>>

[5] M_A_CUk0 >>>
[5] M_A_CUk00 >>>
[5] M_A_CUk1 >>>
[5] M_A_CUk01 >>>

[5] M_A_CK00 >>>
[5] M_A_CK01 >>>

[5] M_A_CS#0 >>>
[5] M_A_CS#1 >>>

[5] M_A_ODT0 >>>
[5] M_A_ODT1 >>>

[99] CPU_SMB_SDA_DOR >>>
[99] CPU_SMB_SCL_DDR >>>

[5,13] SM_DRAMRST# >>>

M_A_ACT N >>>
M_A_ALERT_N >>>
M_A_PARITY >>>

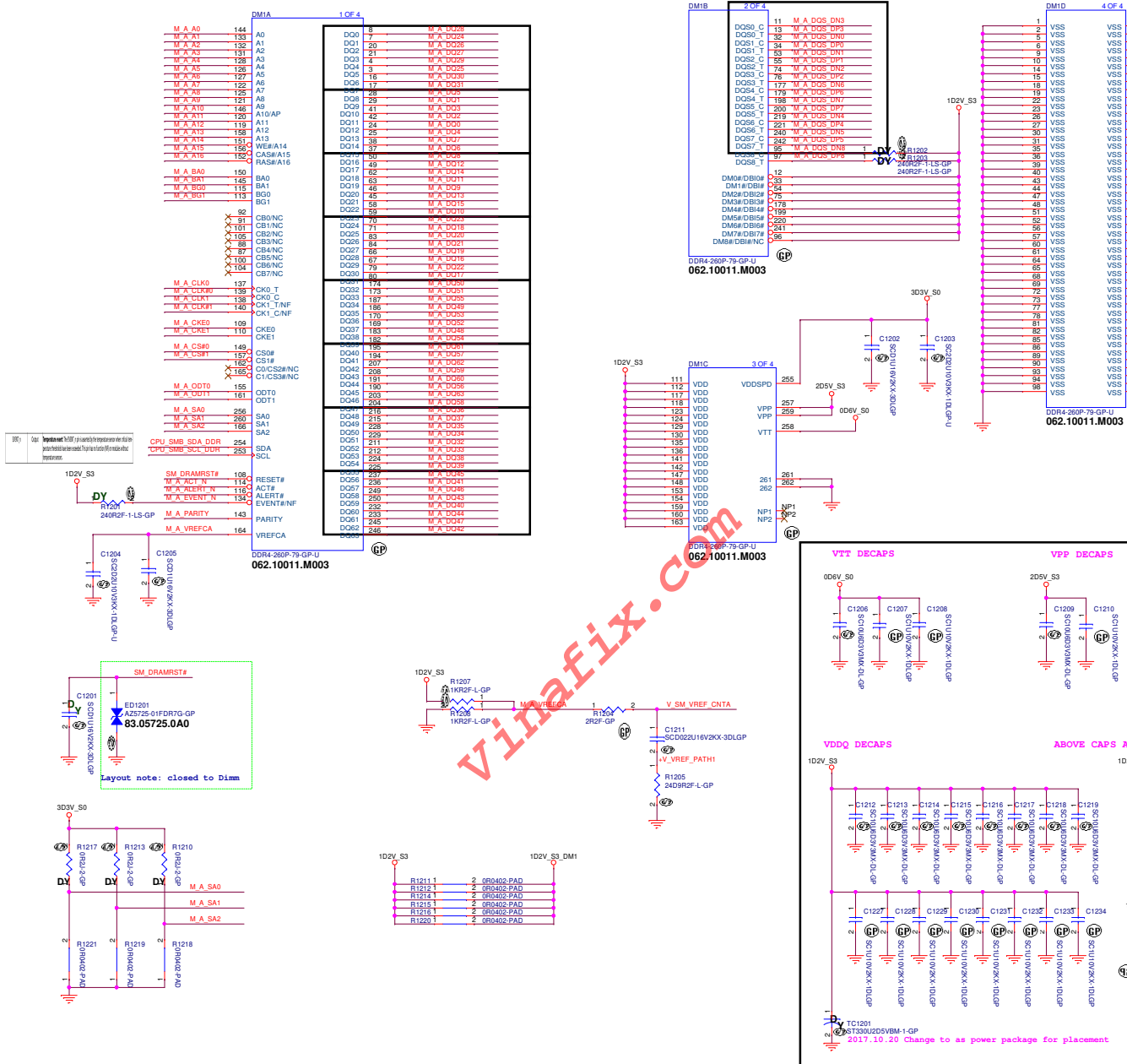
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M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ5
M_A_DQ6
M_A_DQ7
M_A_DQ8
M_A_DQ9
M_A_DQ10
M_A_DQ11
M_A_DQ12
M_A_DQ13
M_A_DQ14
M_A_DQ15
M_A_DQ16
M_A_DQ17
M_A_DQ18
M_A_DQ19
M_A_DQ20
M_A_DQ21
M_A_DQ22
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M_A_DQ28
M_A_DQ29
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M_A_DQ32
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M_A_DQ50
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M_A_DQ53
M_A_DQ54
M_A_DQ55
M_A_DQ56
M_A_DQ57
M_A_DQ58
M_A_DQ59
M_A_DQ60
M_A_DQ61
M_A_DQ62
M_A_DQ63

M_A_DQS_DN[7:0] <<< M_A_DQS_DN0
M_A_DQS_DN1
M_A_DQS_DN2
M_A_DQS_DN3
M_A_DQS_DN4
M_A_DQS_DN5
M_A_DQS_DN6
M_A_DQS_DN7

M_A_DQS_DP[7:0] <<< M_A_DQS_DP0
M_A_DQS_DP1
M_A_DQS_DP2
M_A_DQS_DP3
M_A_DQS_DP4
M_A_DQS_DP5
M_A_DQS_DP6
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[5] V_SM_VREF_CNTA >>>

```



This recommendation assumes a 2CH, 1DPC (2 connector) implementation of SO-DIMMs.

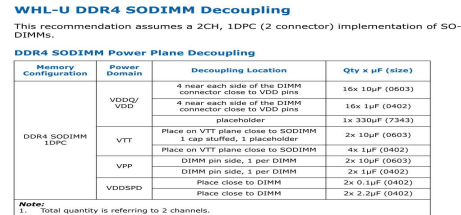
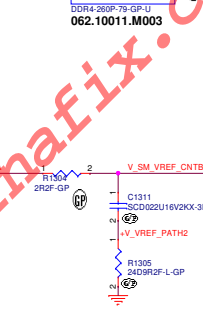
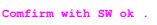
Memory Configuration	Power Domain	Decoupling Location	Qty x Pf (size)
DDR4 SODIMM 16GB	VDDQ/ VDD	4 near each side of the DIMM connector close to VDD pins	16x 1uPf (0603)
		4 near each side of the DIMM connector close to VDD plane placeholder	16x 1uPf (0402)
	VTT	Place on VTT pins close to SODIMM 1 cap stuffed, 1 placeholder	1x 330uF (7843)
		Place on VTT pins close to SODIMM 2x 100nF	2x 100uF (0603)
	VPP	DIMM pin side, 1 per DIMM	2x 10uF (0603)
		DIMM pin side, 1 per DIMM	2x 1uF (0402)
	VPP	Place close to DIMM	2x 0.1uF (0402)
	VDDSP5SD	Place close to DIMM	2x 2.2uF (0402)

**Note:**  
 \* Total quantity is referring to 2 channels.

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Title			
<b>DDR (DDR4-CHA)</b>			
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[5] V\_SM\_VREF\_CNTB >>>\_\_\_\_\_



(Blanking)

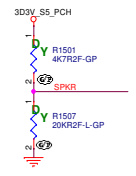
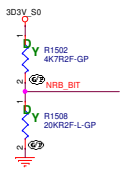
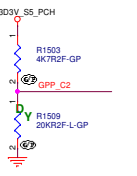
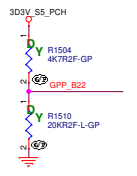
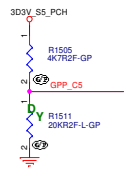
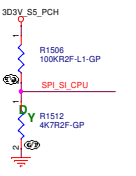
[vinafix.com](http://vinafix.com)

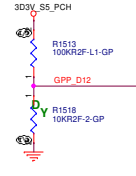
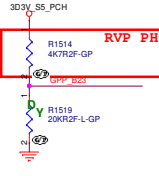
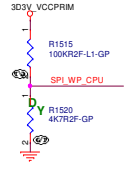
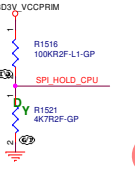
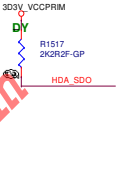
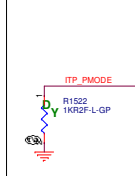
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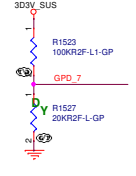
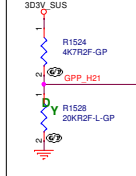
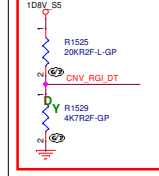
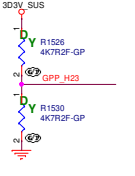
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>(Reserved)_SODIMM _SODIMM4</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
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Main Func = PCH

[19.27] SPKR <<<-  
[20] NRB\_BIT <<<-  
[18.68.99] SPI\_SL\_CPU <<<-  
[18.68.99] SPI\_WP\_CPU <<<-  
[18.68] SPI\_HOLD\_CPU <<<-  
[18] GPP\_C2 <<<-  
[6.99] CFG3 <<>>  
[6.99] CFG4 <<>>  
[15.21] GPD\_7 <<<-  
  
[20] GPP\_D12 >>>-  
[18] GPP\_B23 >>>-  
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[21] GPP\_H21 >>>-  
[21] GPP\_H23 >>>-  
[6.99] ITP\_PMODE >>>-  
[19] HDA\_SDO >>>-  
[18] GPP\_C5 >>>-  
[20] GPP\_B22 >>>-  
[20.61] CNV\_RGL\_DT >>>-

Description	Top Swap Override	No Reboot	TLS Confidentiality	BOOT BIOS STRAP (BBS)	ESPI OR LPC	BOOT HALT
GPIO	GPP_B14 / SFER / TIME_SYNC1 / GSP10_CS#	GPP_B18	GPP_C2	GPP_B22	GPP_C5	SPI0_MOSI
						
LOW	Disable (Default)	Disable (Default)	Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)	SPI SELECTED. (DEFAULT)	LPC SELECTED	
HIGH	Enable	Enable	Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.	LPC SELECTED FOR SYSTEM FLASH	HIGH: ESPI IS SELECTED FOR EC	This strap should sample HIGH.
	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-down.	20 K± 30% internal pull-up.

Description	JTAG ODT DISABLE	EXI BOOT STALL BYPASS	CONSENT STRAP	A0 PERSONALITY STRAP	Flash Descriptor Security Override	DFXTESTMODE
GPIO	GPP_D12	GPP_B23	SPI0_IO2	SPI0_IO3	HDA_SDO/12S0_TXD	ITP_PMODE
						
LOW	JTAG ODT DISABLED	ENABLED (BSSB 2+2)	ENABLED	ENABLED	Enable security measures, and security is not overridden	DFXTESTMODE DISABLE (DEFAULT)
HIGH	JTAG ODT ENABLED	DISABLED (BSSB 4 WIRE)	DISABLED	DISABLED	Disable security measures, and security is overridden	DFXTESTMODE ENABLE
	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-up	20 K± 30% internal pull-down.	20 K± 30% internal pull-up

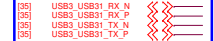
Description	RING OSCILLATOR BYPASS	XTAL FREQUENCY SELECT	M.2 CNVi Mode Select	MAF/SAF STRAP
GPIO	GPD7	GPP_H21	GPP_F6 / CNV_RGL_DT	GPP_H23
				
LOW	XTAL INPUT IS SINGLE ENDED	38.4/19.2MHZ (DEFAULT)	Integrated CNVi enabled	MAF ENABLE
HIGH	XTAL INPUT IS ATTACHED	24MHZ	Integrated CNVi disabled	SAF ENABLE

Main Func = PCH

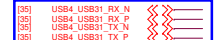
#543016:  
220 nF nominal capacitors are recommended for Gen 3.  
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

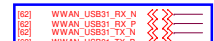
USB3.1 PORT3



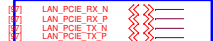
USB3.1 PORT4



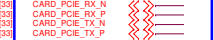
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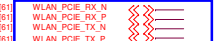
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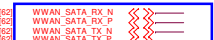
CARD



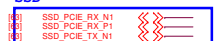
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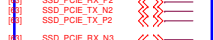
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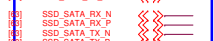
FP



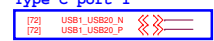
USB charger



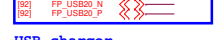
USB2.0 port1



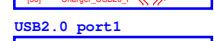
CAMERA



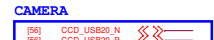
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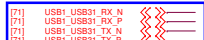
USH



BT



USB3.1 PORT3



LAN



WLAN



CARDREADER



WWAN



SSD



FP



USB charger



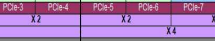
USB2.0 port1



CAMERA



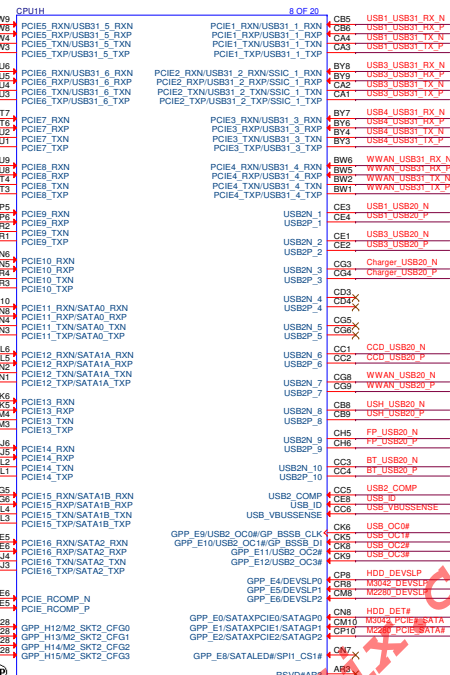
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USH



BT

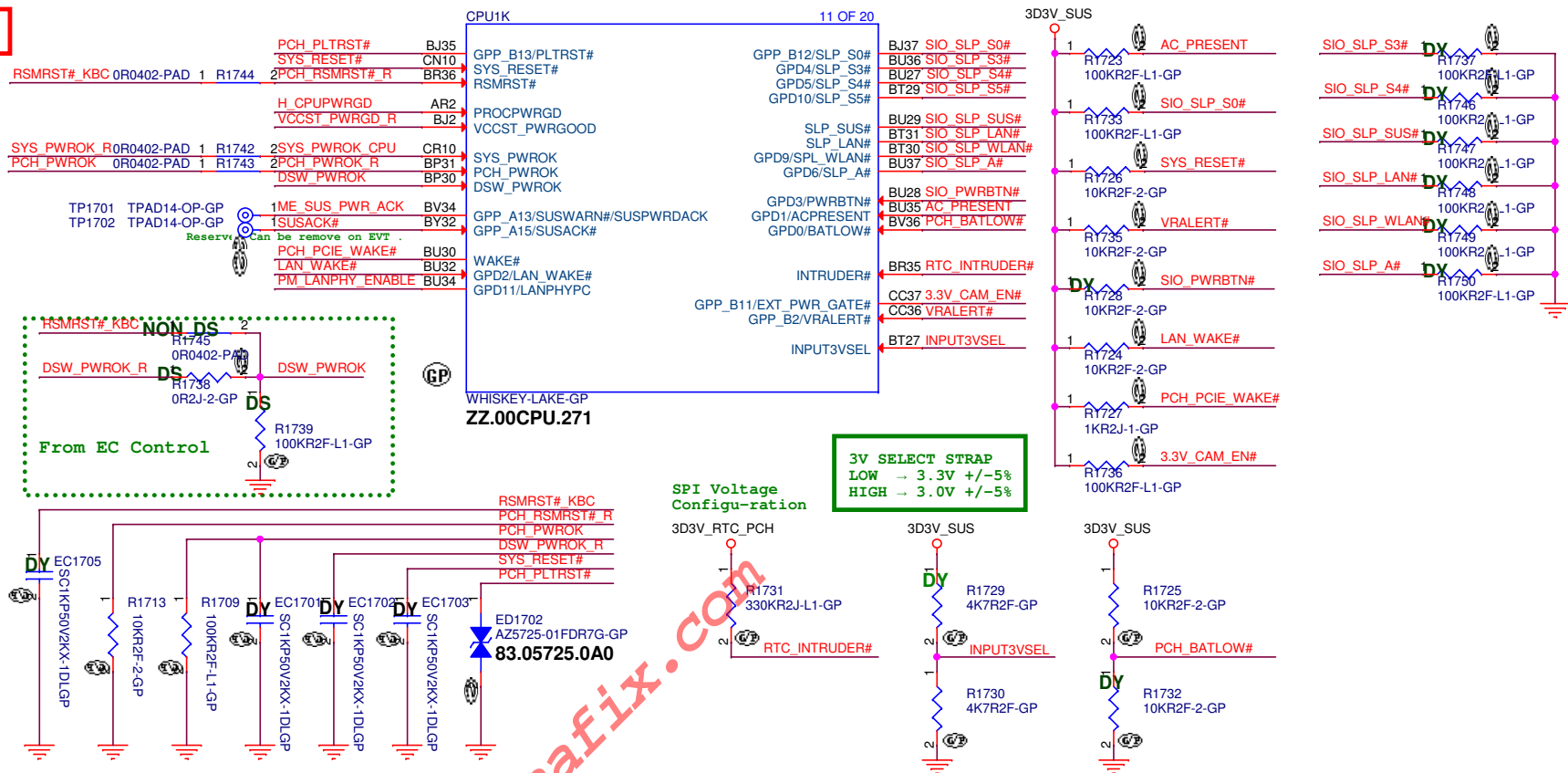


Layout Note:

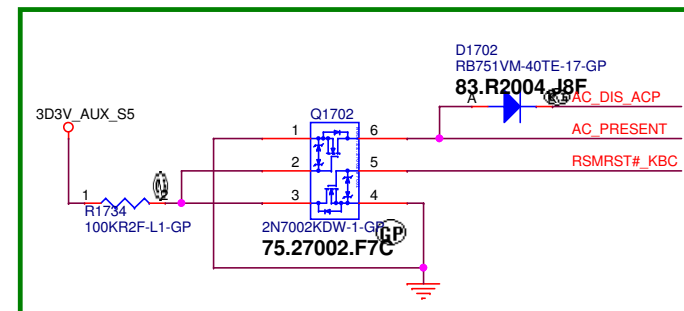
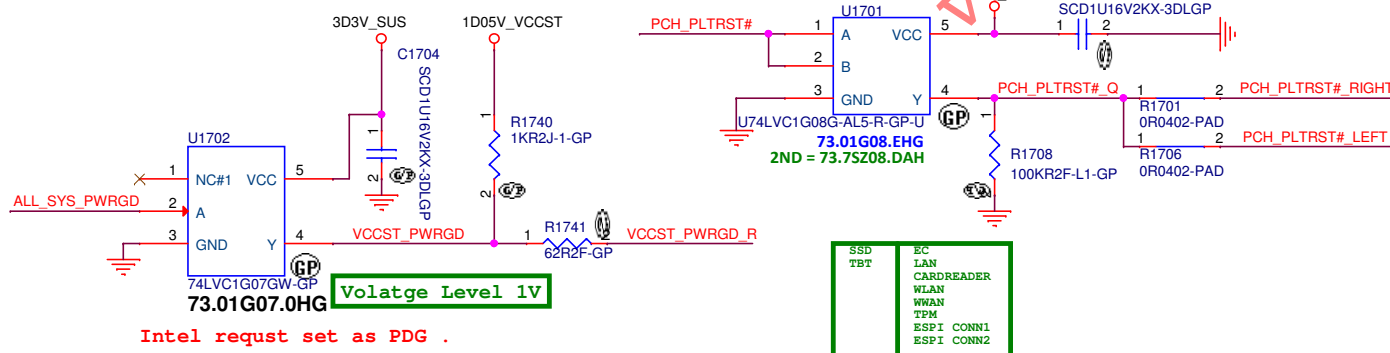
- 1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
- Note: Must maintain low DC resistance (R<0.1 ohm).
- 2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

		PCIe Controller 1				PCIe Controller 2				PCIe Controller 3				PCIe Controller 4			
		SATA0-3 (SATA)				SATA4-7 (SATA)				SATA8-11 (SATA)				SATA12-15 (SATA)			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Canon Lake U PCH-LP	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0	USB3.1/3.0
	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1	Port 1
	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2	Port 2
	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3	Port 3
		X4				X2				X2				X2			
		X4				X2				X2				X2			
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		X4															

[24,40,52,53,54]	SIO_SLP_SUS#	<<<=====
[68]	SIO_SLP_S5#	<<<=====
[40,51,68]	SIO_SLP_S4#	<<<=====
[24,40,51,68,71]	SIO_SLP_S3#	<<<=====
[68]	SIO_SLP_A#	<<<=====
[40,54,68,91]	SIO_SLP_S0#	<<<=====
[40]	SIO_SLP_WLAN#	<<<=====
[40]	SIO_SLP_LAN#	<<<=====
[68,99]	SYS_RESET#	<<<=====
[24]	DSW_PWROK_R	>>>=====
[46]	PCH_PWROK	>>>=====
[24]	SYS_PWROK_R	>>>=====
[24,99]	SIO_PWRBTN#	>>>=====
[24]	AC_PRESENT	<<<=====
[24,97]	LAN_WAKE#	<<<=====
[24,62,71]	PCH_PCIE_WAKE#	<<<=====
[97]	PM_LANPHY_ENABLE	<<<=====
[18,24]	RTRCST_ON	>>>=====
[24,64,99]	RSMRST#_KBC	>>>=====
[24]	ALL_SYS_PWRGD	>>>=====
[33,61,62,91,97]	PCH_PLTRST#_RIGHT	<<<=====
[63,71,99]	PCH_PLTRST#_LEFT	<<<=====
[21,24,40,54,91]	CPU_C10_GATE#	<<<=====
[3]	H_CPUUPWRGD	<<<=====
[40]	3.3V_CAM_EN#	>>>=====
[44]	AC_DIS_ACP	>>>=====



CheckList 10K ,Reserve PL for RTC rst test



## <Core Design>



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Title	<b><i>CPU_ (POWER MANAGEMENT)</i></b>
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Size Custom	Document Number <b><i>Bandon / NorthBay 13"</i></b>	Rev <b><i>X00</i></b>
Date: Friday, February 15, 2019	Sheet 17 of 106	







# Main Func = PCH

[27] HDA\_SDIO <<< —  
[27] HDA\_SDOOUT\_CODEC <<< —  
[27] HDA\_SYNC\_CODEC <<< —  
[27] HDA\_BITCLK\_CODEC <<< —  
[15] HDA\_SDO <<< —

[66] CONTACTLESS\_DET# >>> —

[56] CAM\_MIC\_CBL\_DET# >>> —

[29] SPK\_DET# >>> —

[33] HOST\_SD\_WP# >>> —

[27] AUD\_PWR\_EN <<< —

[68] ME\_FWP\_PCH <<< —

[15,27] SPKR <<< —

[61] CLKREQ\_CNV >>> —  
[61] CNV\_RF\_RESET# >>> —

[65] KB\_DET# <<< —

[62] WWAN\_GPIO\_WAKE# <<< —

[71] TBT\_CIO\_PLUG\_EVENT# <<< —

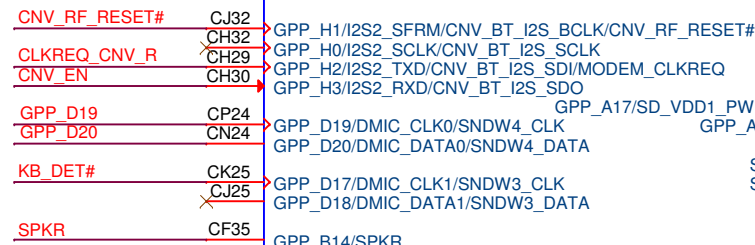
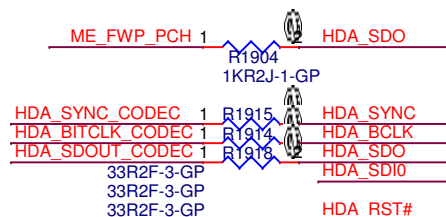
[56] DMIC\_SDA\_CODEEC\_CPU <<< —

[56] DMIC\_SCL\_CODEEC\_CPU <<< —

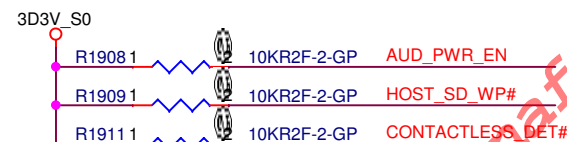
[62] ANT\_CONFIG >>> —

[61] CNV\_EN <<< —

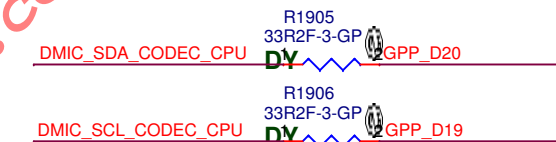
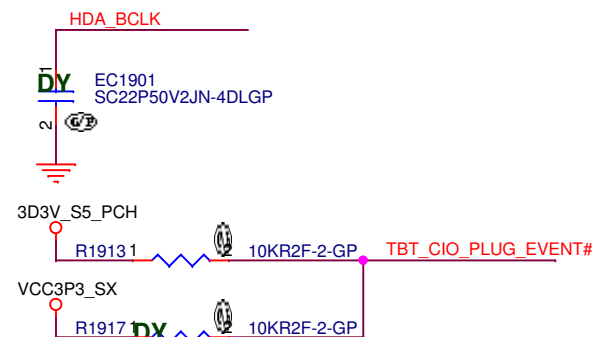
[27] HDA\_RST# <<< —



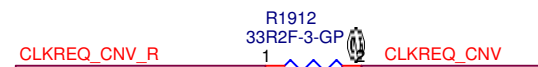
WHISKEY-LAKE-GP  
ZZ.00CPU.271



GPI00.5 change to 1.8V



Reserve for Dmic connect to PCH



<Core Design>



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Title

CPU (AUDIO/SDIO/SDXC)

Size  
A4

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# Main Func = PCH

[68] CPU\_UART2\_TXD <<< <<<  
[68] CPU\_UART2\_RXD <<< <<<  
[55] CPU\_I2C\_SDA\_TS <<< <<<  
[55] CPU\_I2C\_SCL\_TS <<< <<<  
[65] CPU\_I2C\_SDA\_TP <<< <<<  
[65] CPU\_I2C\_SCL\_TP <<< <<<

[69,70] CPU\_I2C\_SDA\_SENSOR <<< <<<  
[69,70] CPU\_I2C\_SCL\_SENSOR <<< <<<

[62] CPU\_I2C\_SDA\_GNSS <<< <<<  
[62] CPU\_I2C\_SCL\_GNSS <<< <<<

[69] GSEN\_INT1 <<< <<<  
[70] LNG2DMTR\_INT1 <<< <<<

[24] NB\_MODE# <<< <<<  
[24] LID\_CL#\_NB\_R <<< <<<

[24] LID\_CL#\_TAB\_R <<< <<<  
[15,20] NRB\_BIT <<< <<<

[91] TPM\_PIRQ# <<< <<<  
[40] PCH\_3.3V\_TS\_EN <<< <<<

[15] GPP\_B22 <<< <<<  
[55] TS\_INT# <<< <<<

[24] SIO\_EXT\_WAKE# <<< <<<  
[55] LCD\_CBL\_DET# <<< <<<

[61] CNV\_BRI\_RSP <<< <<<  
[15,61] CNV\_RGI\_DT <<< <<<  
[61] CNV\_BRI\_DT <<< <<<  
[61] CNV\_RGI\_RSP <<< <<<

[15,20] NRB\_BIT <<< <<<  
[15] GPP\_D12 <<< <<<

[56] IR\_CAM\_DET# <<< <<<  
[62] WWAN\_FULL\_PWR\_EN# <<< <<<

[54] PRIM\_CORE\_OPT\_DIS <<< <<<  
[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

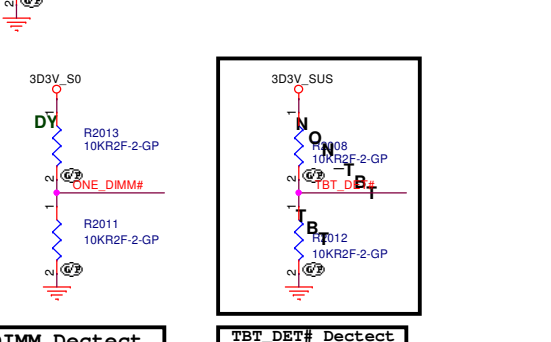
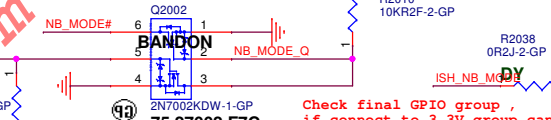
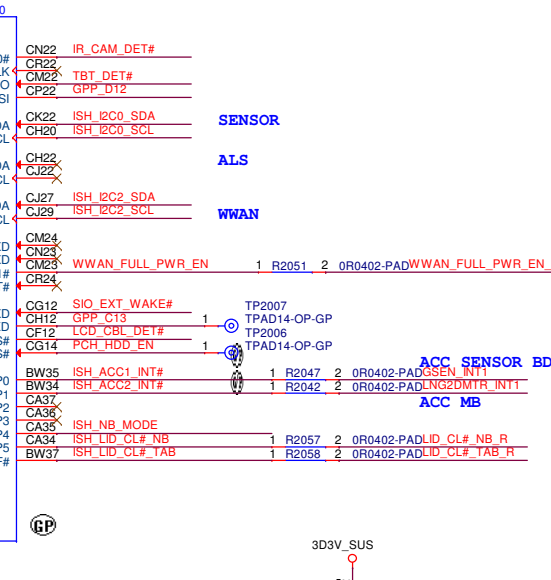
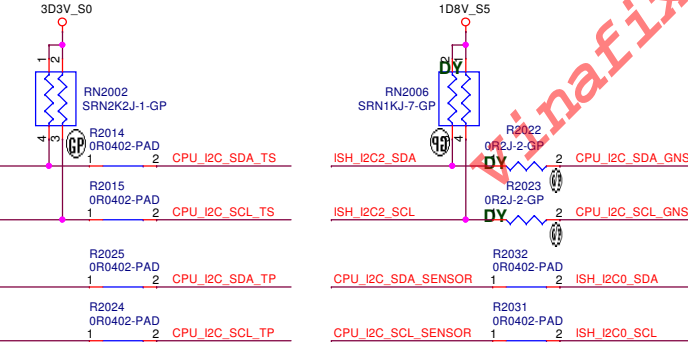
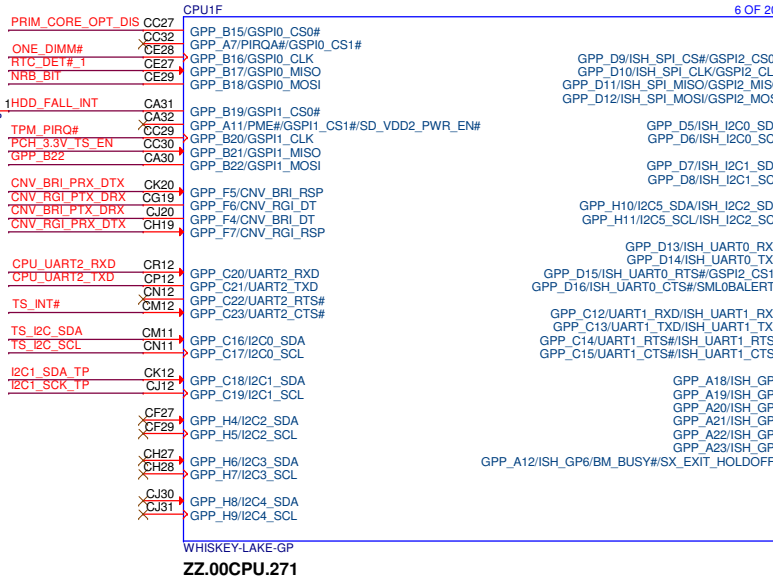
[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

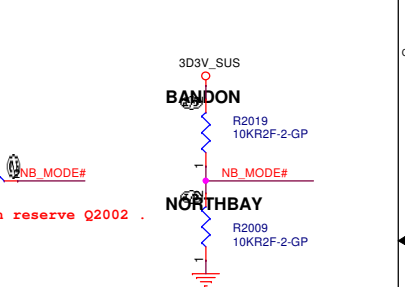
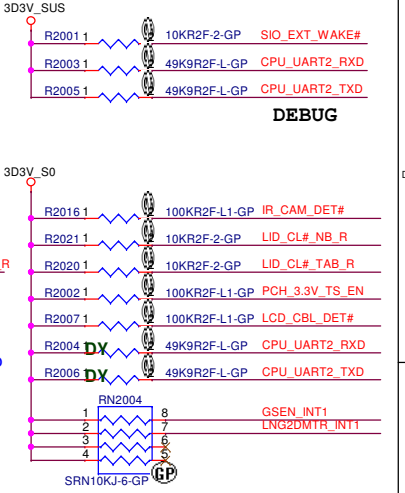
[18,25] RTC\_DET# <<< <<<

[18,25] RTC\_DET# <<< <<<

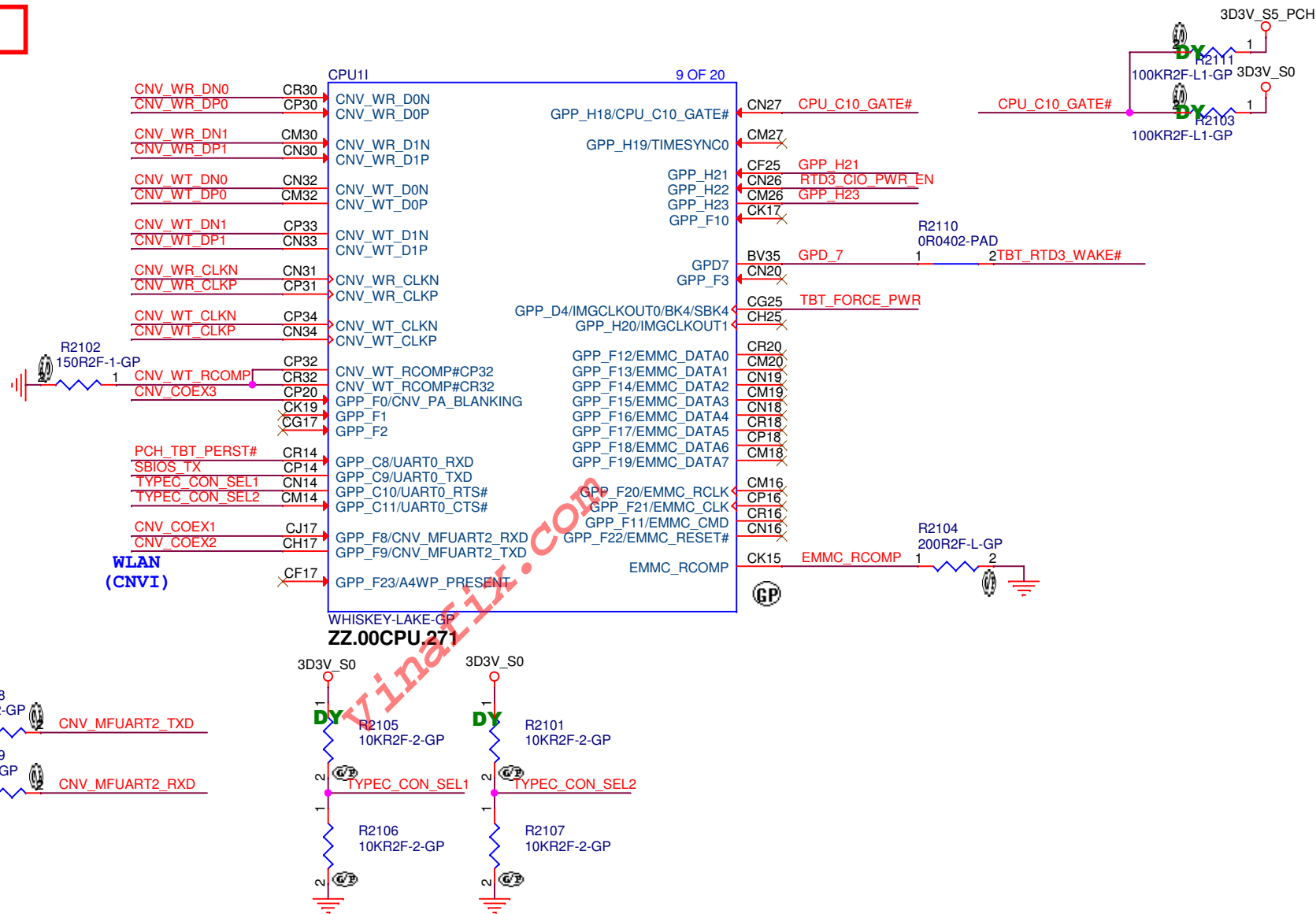


DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

TBT_DET# Detect	
HIGH	NON TBT
LOW	TBT



[61]	CNV_WR_DN0	>>>	_____
[61]	CNV_WR_DP0	>>>	_____
[61]	CNV_WR_DN1	>>>	_____
[61]	CNV_WR_DP1	>>>	_____
[61]	CNV_WR_CLKN	>>>	_____
[61]	CNV_WR_CLKP	>>>	_____
[61]	CNV_WT_DN0	>>>	_____
[61]	CNV_WT_DP0	>>>	_____
[61]	CNV_WT_DN1	>>>	_____
[61]	CNV_WT_DP1	>>>	_____
[61]	CNV_WT_CLKN	>>>	_____
[61]	CNV_WT_CLKP	>>>	_____
[61,62]	CNV_COEX3	<<<	_____
[62,68]	SBIOS_TX	<<<	_____
[24,40,54,91]	CPU_C10_GATE#	<<<	_____
[71]	TBT_FORCE_PWR	<<<	_____
[71]	PCH_TBT_PERST#	<<<	_____
[61,62]	CNV_MFUART2_TXD	<<<>>>	_____
[61,62]	CNV_MFUART2_RXD	<<<>>>	_____
[15]	GPP_H21	<<<	_____
[15]	GPP_H23	<<<	_____
[15]	GPD_7	<<<	_____
[71]	TBT_RTD3_WAKE#	>>>	_____
[71]	RTD3_CIO_PWR_EN	<<<	_____



Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH



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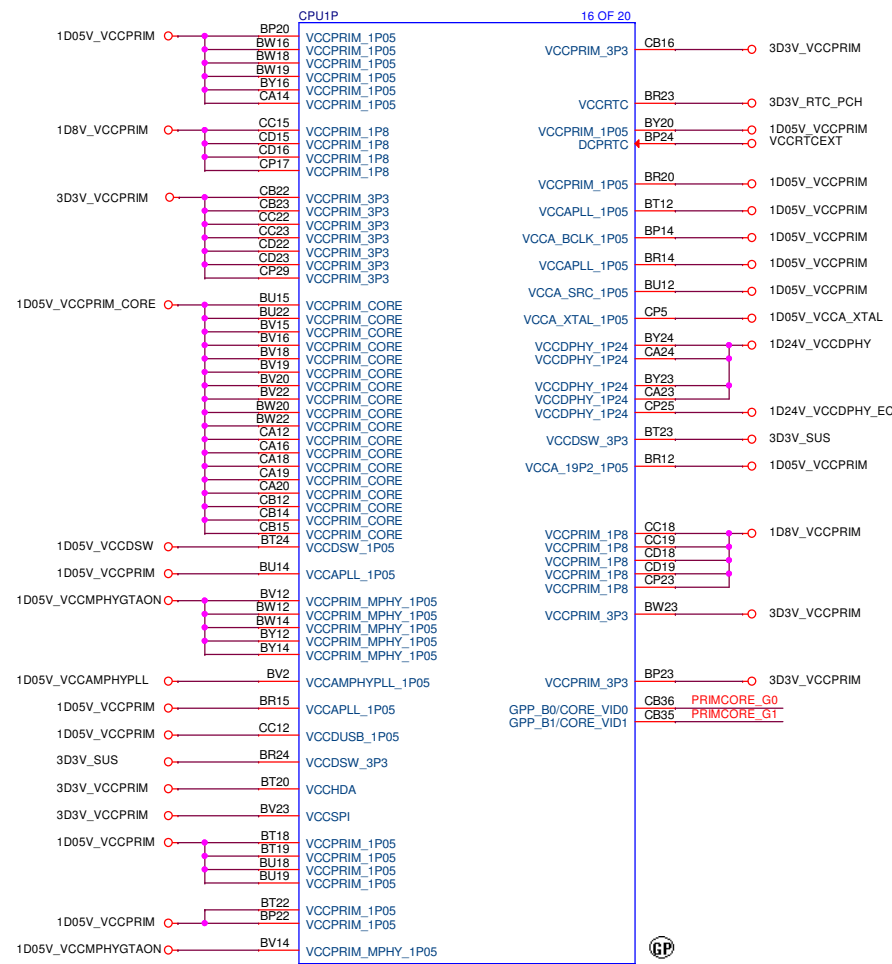
**CPU (POWER1)**

***Bandon / NorthBay 13"***

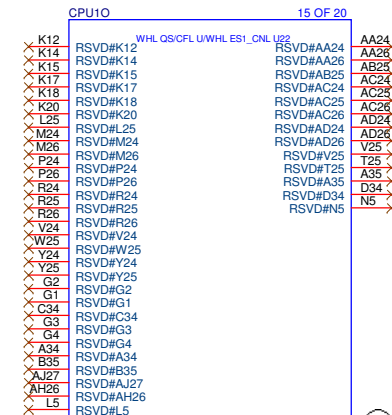
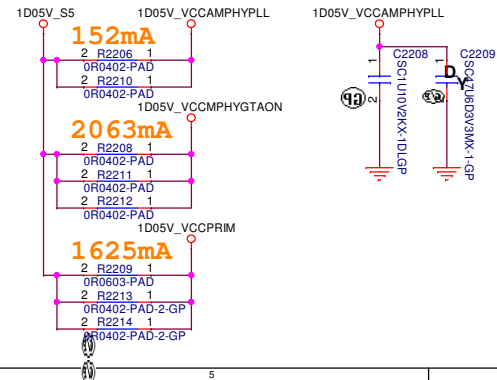
Rev  
**X00**

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```
[54] PRIMCORE_G0    >>>_____
[54] PRIMCORE_G1    >>>_____
```



**Layout Note:**  
22uF:  
C2209 near BV2




Layout Note:  
R2202 near CP5

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Title			
		<b>CPU (RSVD)</b>	
Size A3	Document Number	<b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
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Main Func = PCH

<Core Design>



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Title

**CPU (VSS)**

**Bandon / NorthBay 13"**

Size  
A4

Document Number

Rev  
X00

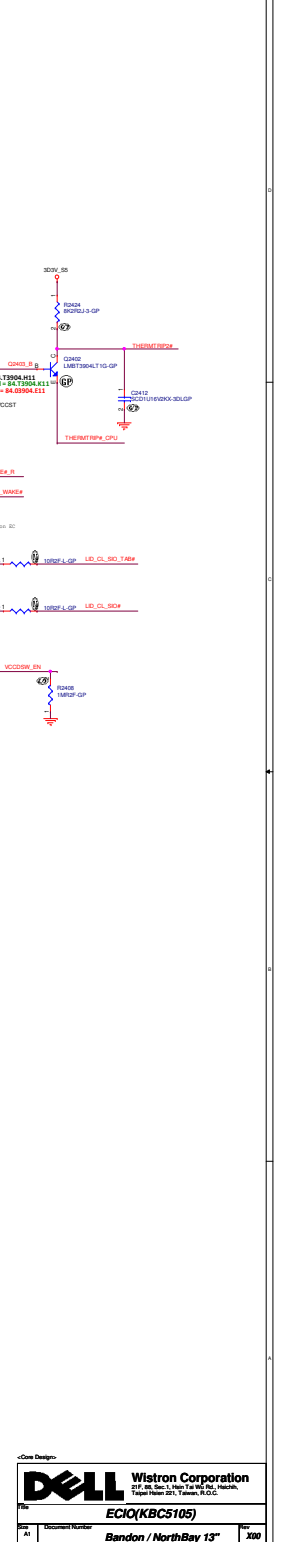
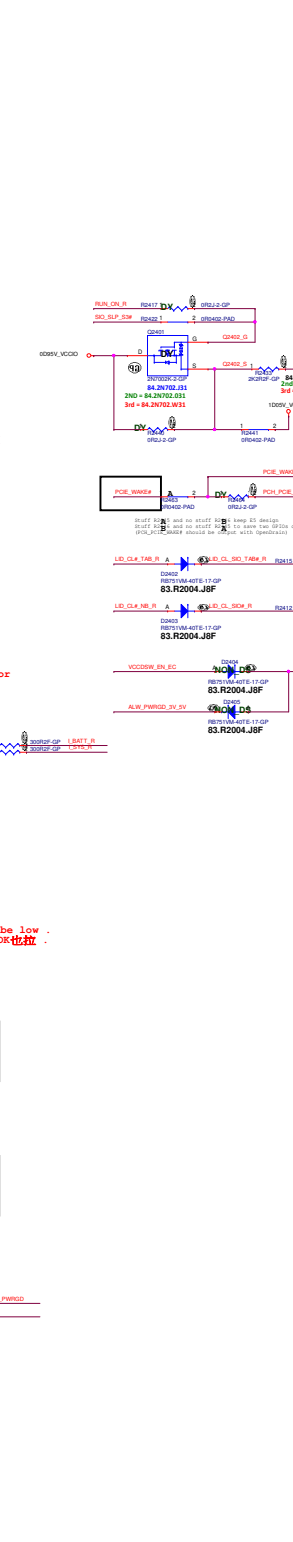
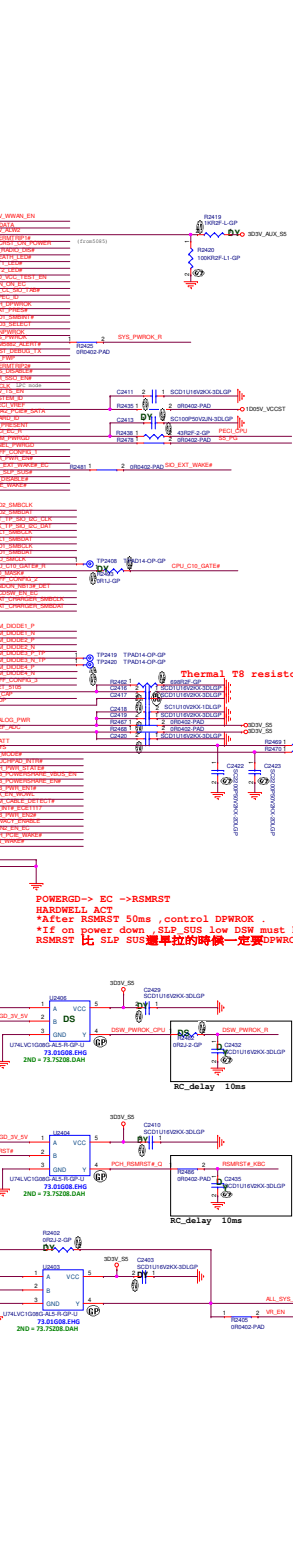
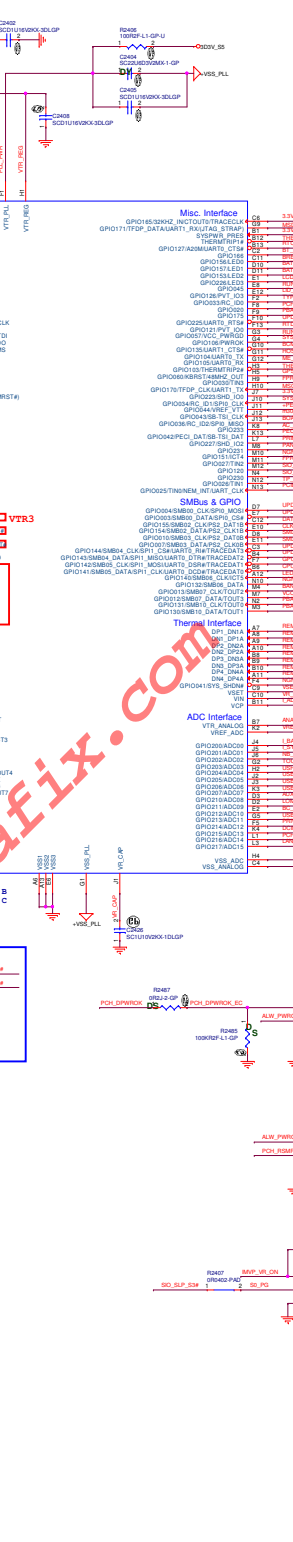
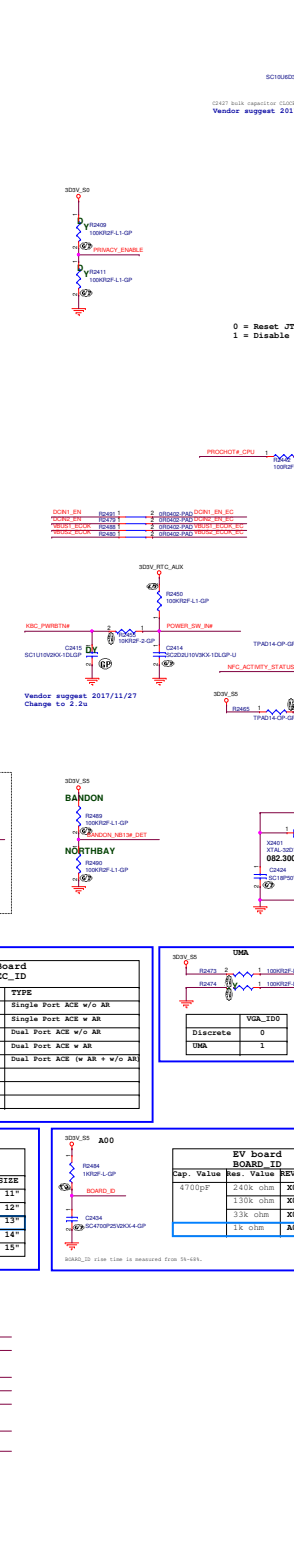
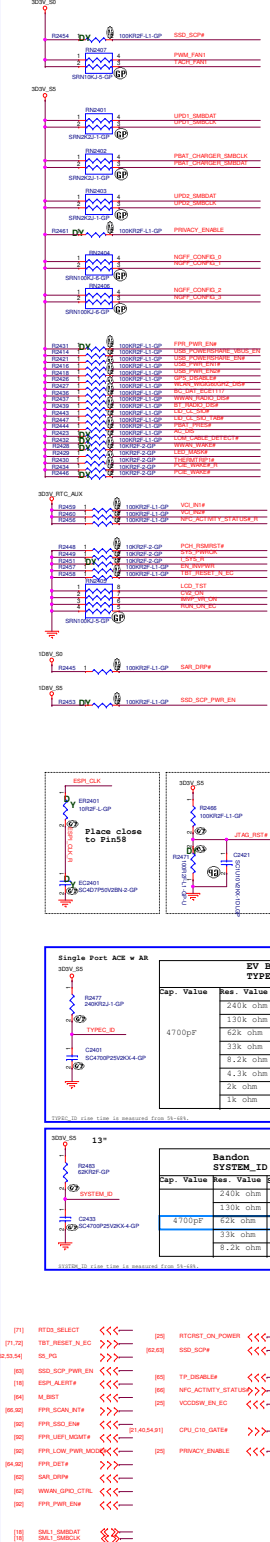
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Main Func = EC

- [1] SERIAL\_MASTER
- [2] SERIAL\_SLAVE
- [3] SERIAL\_SLAVE
- [4] SERIAL\_SLAVE
- [5] SERIAL\_SLAVE
- [6] SERIAL\_SLAVE
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- [100] SERIAL\_SLAVE



## SYSTEM SPI ROM



**X09 design DS3 Non-DS3 with RTC power gating**



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Taipei Hsien 221, Taiwan, R.O.C.

Flash/RTC

**Bandon / NorthBay 13"**

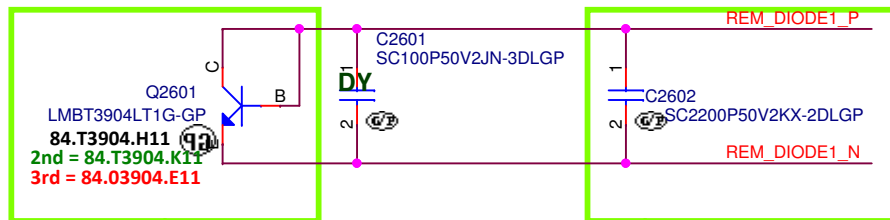
106



# Main Func = Thermal / FAN

[24] REM\_DIODE1\_P  
[24] REM\_DIODE1\_N  
[24] REM\_DIODE2\_P  
[24] REM\_DIODE2\_N

[24] REM\_DIODE4\_P  
[24] REM\_DIODE4\_N  
[24] PWM\_FAN1  
[24] TACH\_FAN1

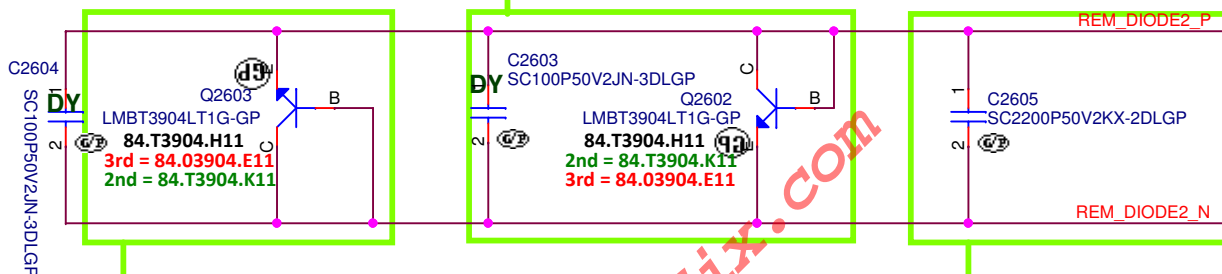


**Layout Note: Place to CPU**

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

**Layout Note: Close to EC**

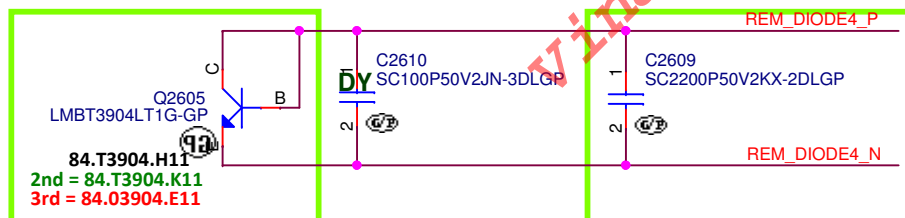
**Layout Note: Close to WWAN/2nd SSD**



**Layout Note: Place to DIMM**

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

**Layout Note: Close to EC**

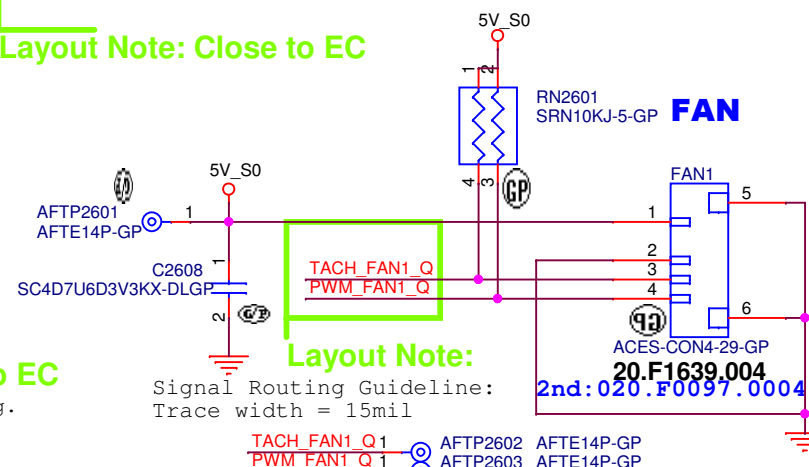
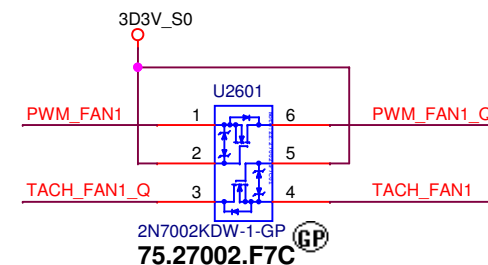


**Layout Note: Place to V.R**

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

**Layout Note: Close to EC**

5105 Channel	Location
DP1/DN1	CPU (Q2601)
DP2/DN2	WWAN (Q2602)
DN2a/DP2a	DDR (Q2603)
DP4/DN4	V.R (Q2605)



**Layout Note:**

Signal Routing Guideline:  
Trace width = 15mil

TACH\_FAN1\_Q 1  
PWM\_FAN1\_Q 1

<Core Design>



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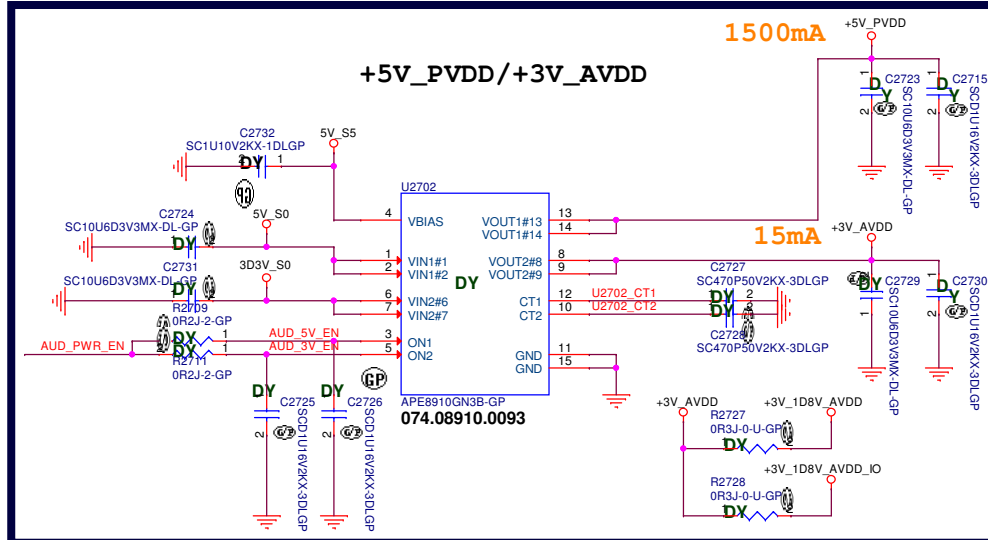
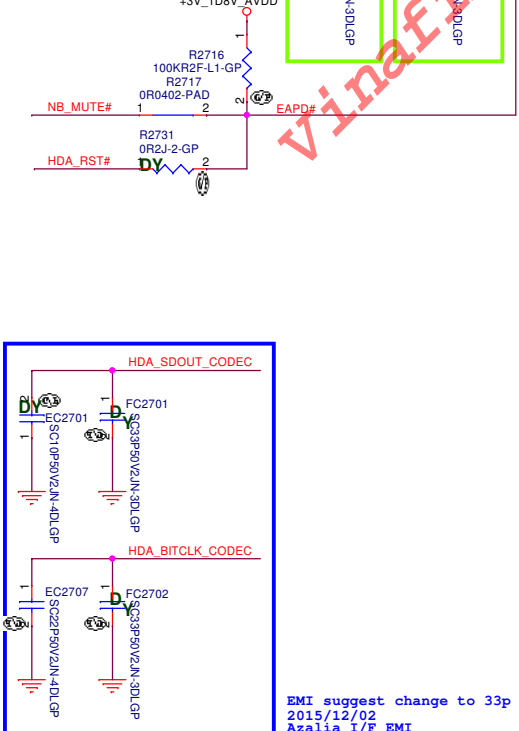
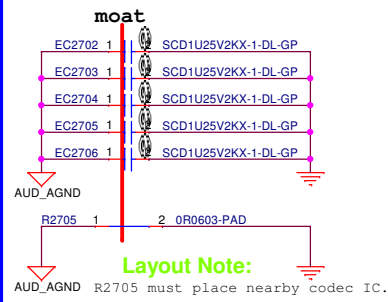
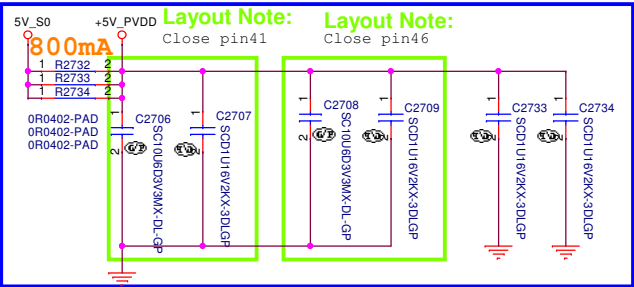
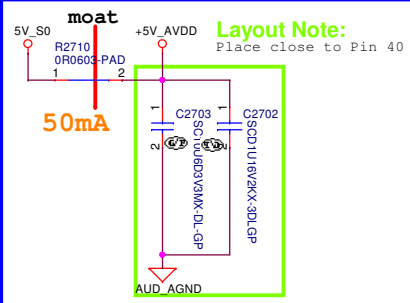
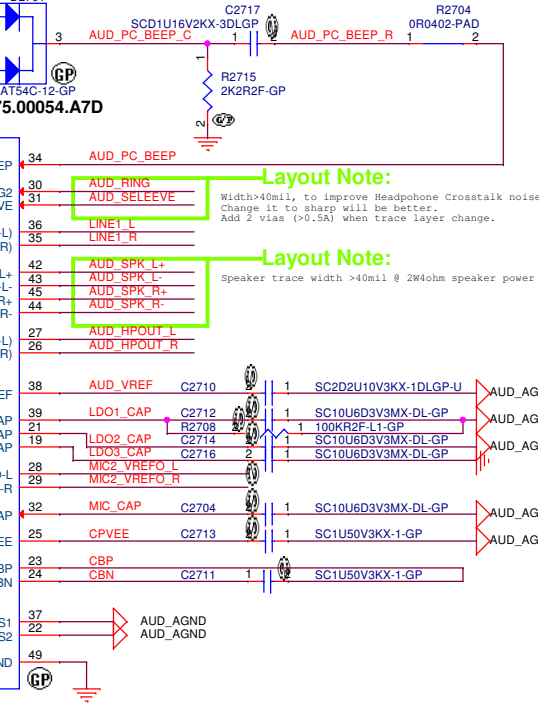
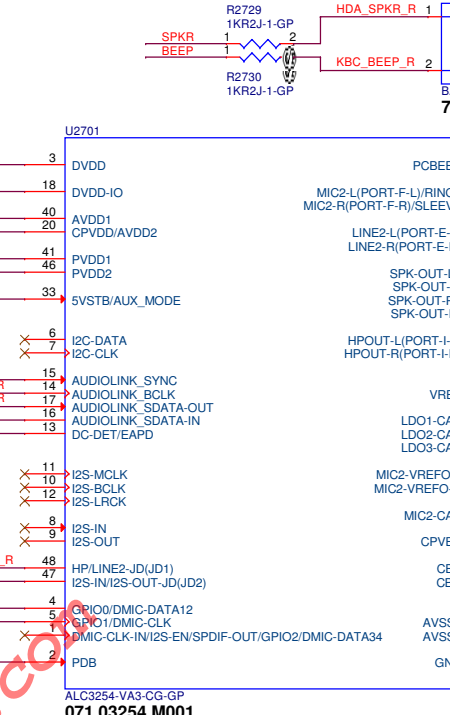
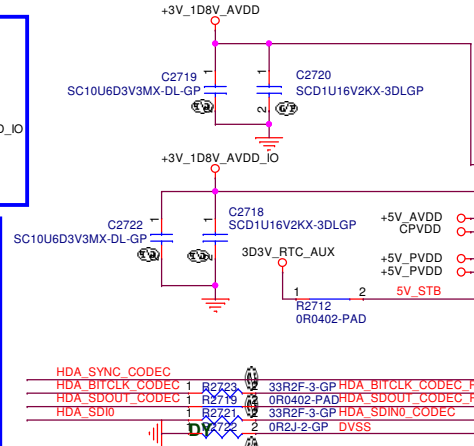
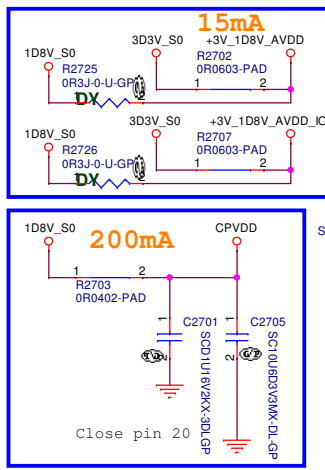
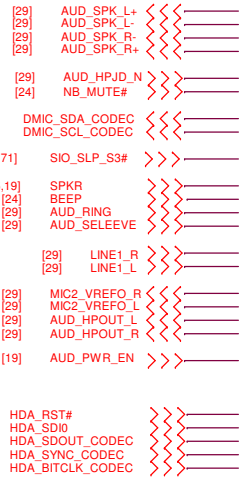
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **INT IO (Thermal/Fan)**

Size A4 Document Number **Bandon / NorthBay 13"** Rev **X00**

Date: Friday, February 15, 2019 Sheet 26 of 106

# Main Func = Audio



<Core Design>

**DELL** Wistron Corporation

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Audio (CodecALC3253)

Size A3 Document Number Bandon / NorthBay 13" Rev X00

Date: Friday, February 15, 2019 Sheet 27 of 106

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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>Audio (RSVD) (Audio AMP)</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 28 of 106




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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Audio (RSVD)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 30 of	106

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<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>LAN (RSVD) (Giga_RTL8151GD)</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 31		of 106	

# Main Func = LAN

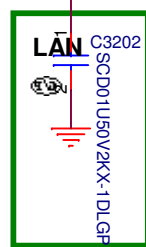
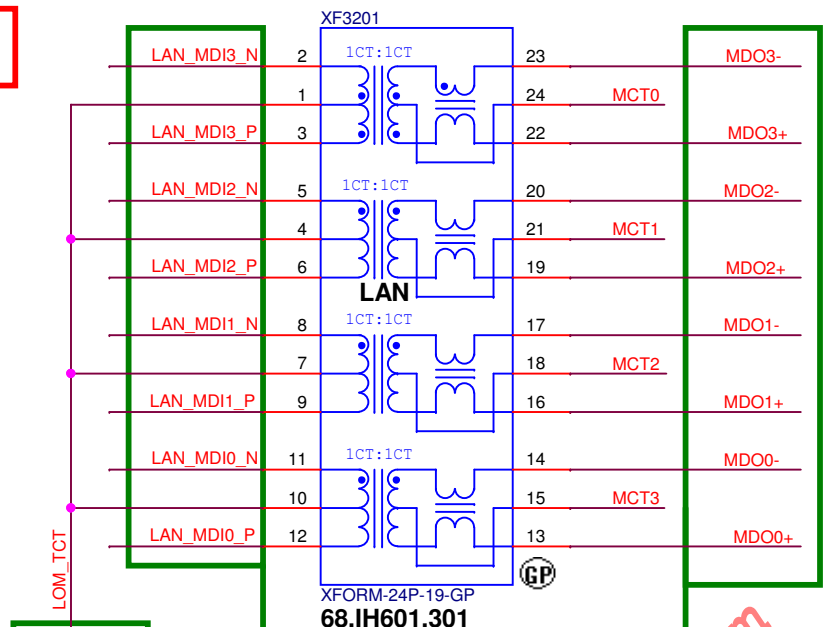
[24,64] LED\_MASK#  
 [97] LAN\_0\_GREEN\_LINK\_N  
 [97] LAN\_1\_AMBER\_ACT\_N

[97] LAN\_MDI0\_P  
 [97] LAN\_MDI0\_N

[97] LAN\_MDI1\_P  
 [97] LAN\_MDI1\_N

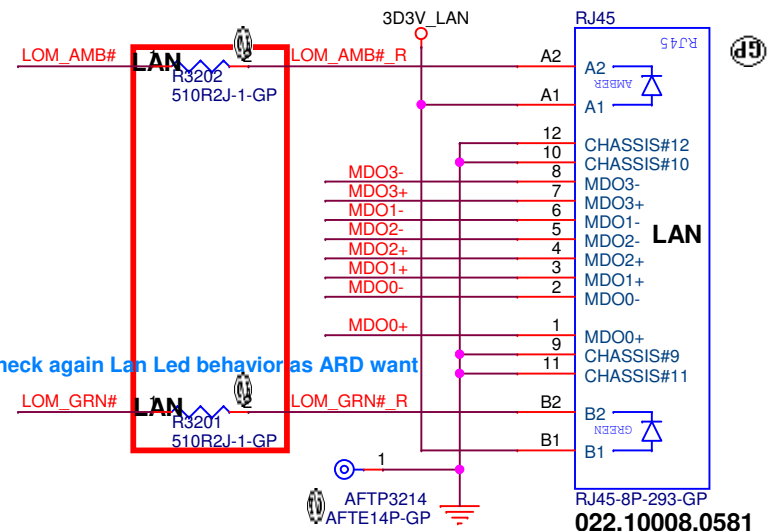
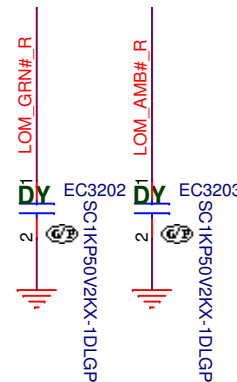
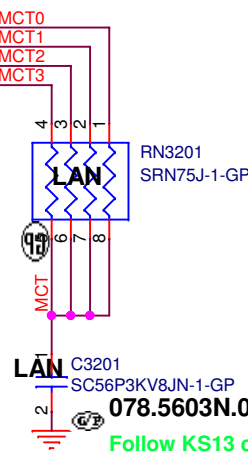
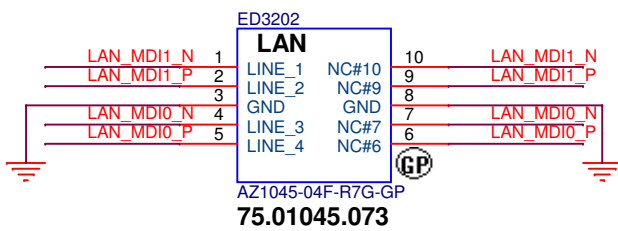
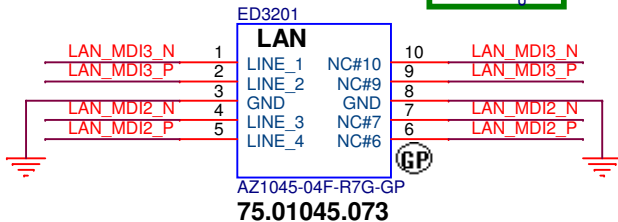
[97] LAN\_MDI2\_P  
 [97] LAN\_MDI2\_N

[97] LAN\_MDI3\_P  
 [97] LAN\_MDI3\_N

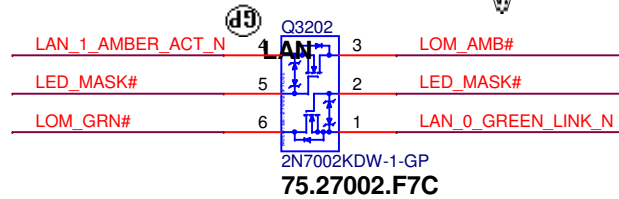


Layout note:  
 30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF



3D3V LAN	1	AFTP3202	AFTE14P-GP
MDO3-	1	AFTP3203	AFTE14P-GP
MDO3+	1	AFTP3204	AFTE14P-GP
MDO2-	1	AFTP3205	AFTE14P-GP
MDO2+	1	AFTP3206	AFTE14P-GP
MDO1-	1	AFTP3207	AFTE14P-GP
MDO1+	1	AFTP3208	AFTE14P-GP
MDO0-	1	AFTP3209	AFTE14P-GP
MDO0+	1	AFTP3210	AFTE14P-GP
LOM GRN#_R	1	AFTP3212	AFTE14P-GP
LOM AMB#_R	1	AFTP3213	AFTE14P-GP



- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

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Title **LAN (RJ45+Transformer)**

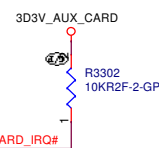
Size A4 Document Number **Bandon / NorthBay 13"** Rev **X00**

Date: Friday, February 15, 2019 Sheet 32 of 106

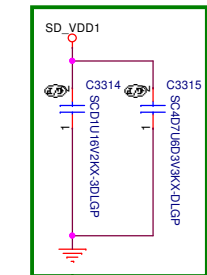
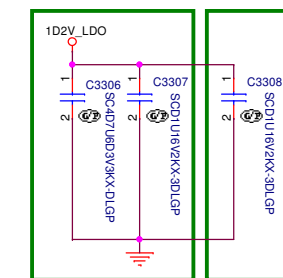
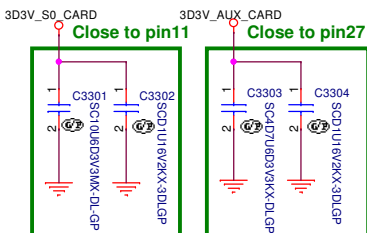


## 3D3V\_S0\_CARD

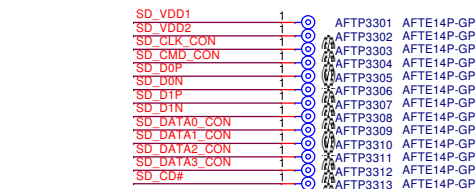
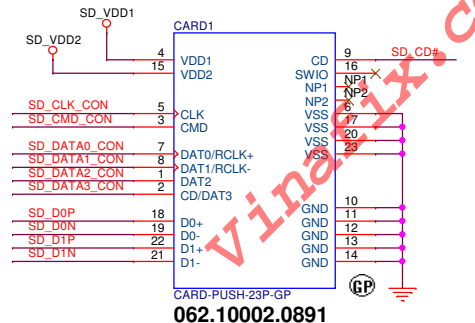
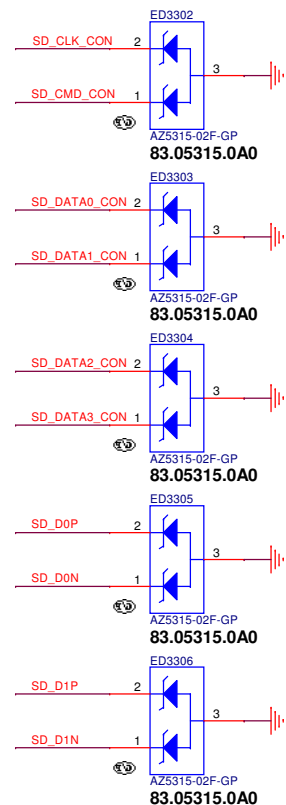
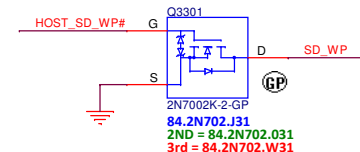
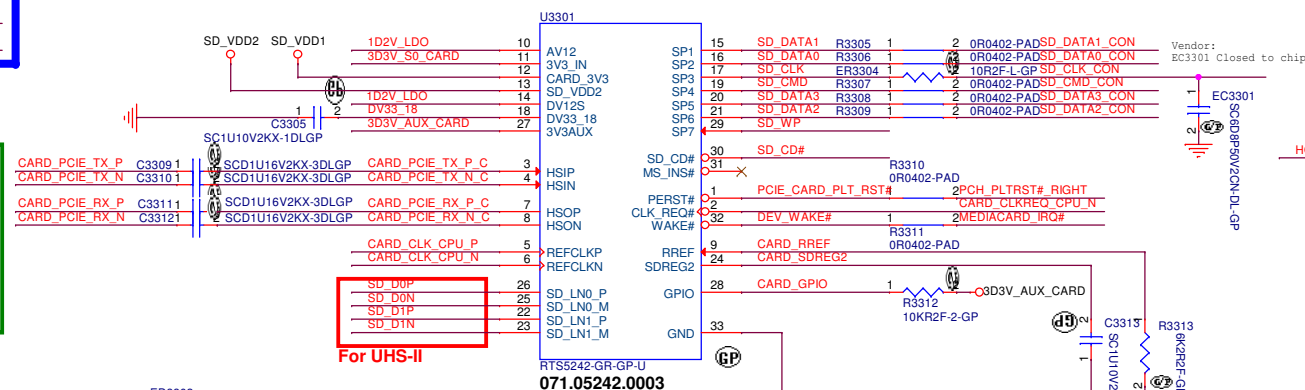
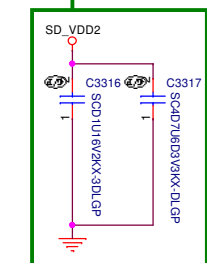
850mA



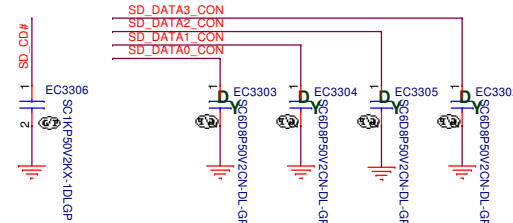
3D3V\_S0\_CARD      3D3V\_AUX\_CARD  
Close to pin11      Close to pin27



**Layout Note:**Close to Card Reader CONN



以上測點不可拉分支型式



## <Core Design>



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Title	<b>CARDREADER (SDIO/SD Conn)</b>
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Size A3	Document Number <b>Banden / North Bay 12"</b>	Rev Y00
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Date: Friday, February 15, 2019 Sheet 33 of 106

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<Core Design>

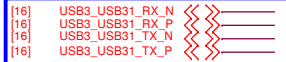
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>USB (RSVD) (USB2.0 CONN)</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 34 of 106

# Main Func = USB 3.0

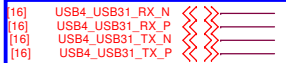
## USB4/USB30-3/USB20-3/PowerShare

EXT Port1 Right Side, Support Power Share

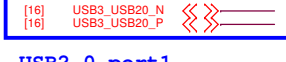
### USB3.1 PORT1



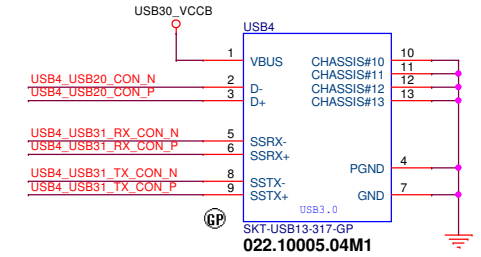
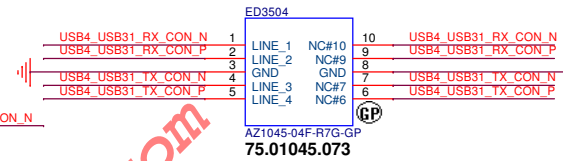
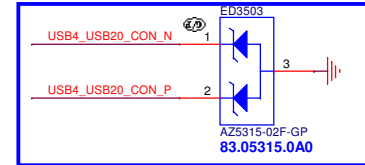
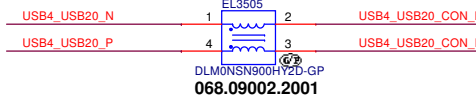
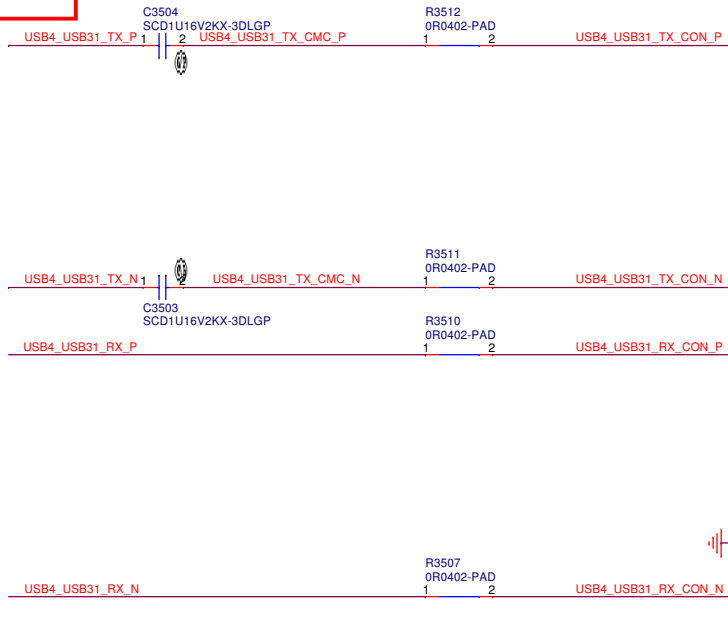
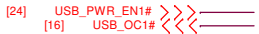
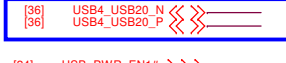
### USB3.1 PORT2



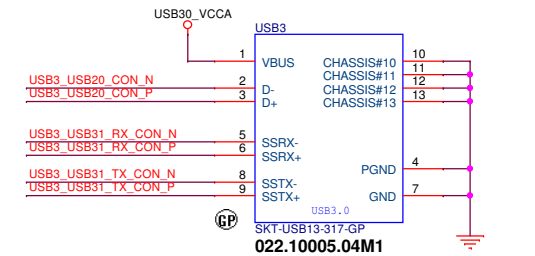
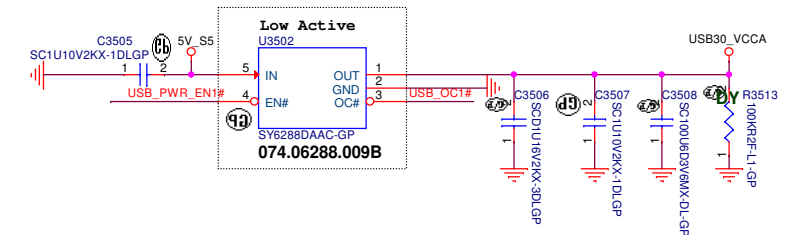
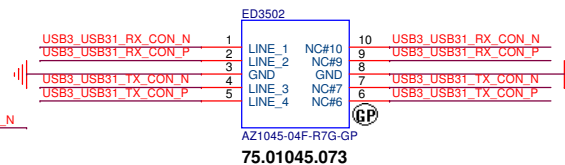
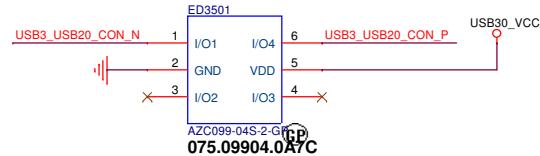
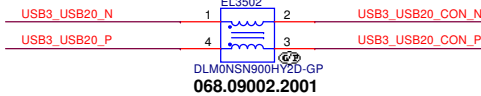
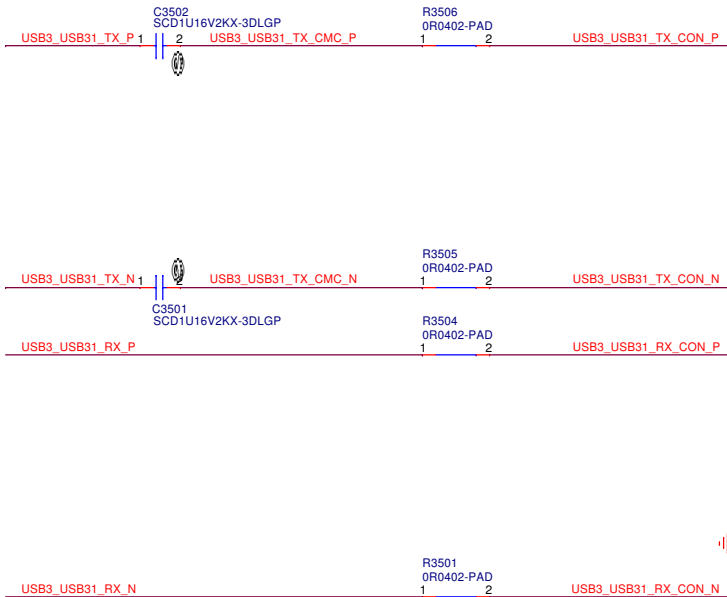
### USB2.0 port2



### USB2.0 port1






## USB3/USB30-3/USB20-2



support power share on the USB3.0 port on the right side of platform

## USB2.0 port2

[35] USB4\_USB20\_N   

[35] USB4\_USB20\_P   

[24] USB\_POWERSHARE\_VBUS\_EN >>> \_\_\_\_\_  
[24] USB\_POWERSHARE\_EN# >>> \_\_\_\_\_

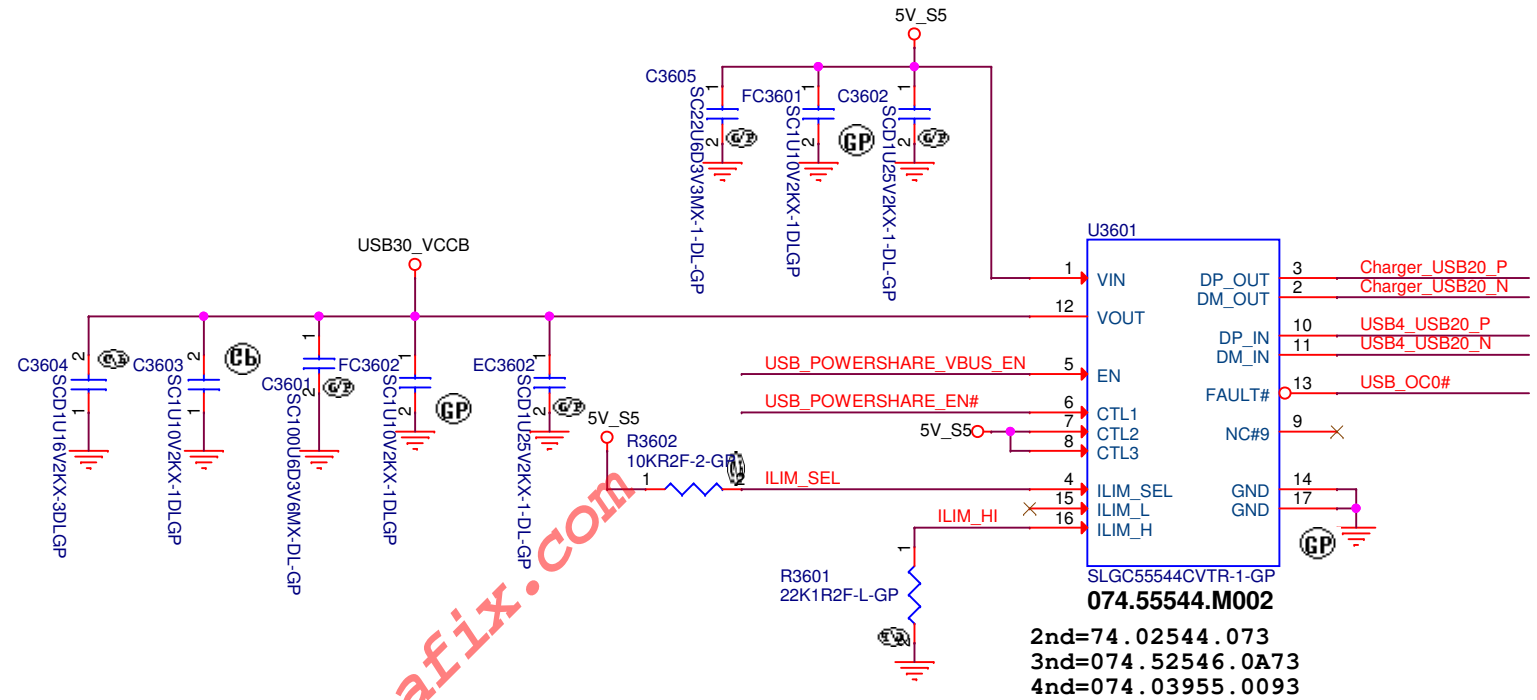
[16] USB\_OC0# <<<\_\_\_\_\_

## USB charger

[16] Charger\_USB20\_N   \_\_\_\_\_  
[16] Charger\_USB20\_P   \_\_\_\_\_

Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570



## <Core Design>



## Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title
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**USB (USB Charger)**

Size  
A4

Document Number
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***Bandon / NorthBay 13"***


Rev  
**X00**

Date: Friday, February 15, 2019

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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>USB (RSVD) (PCIE to USB3.0)</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 37 of 106

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<Core Design>


		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>USB (RSVD)(USB3.0 Redriver)</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 38 of 106



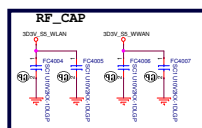
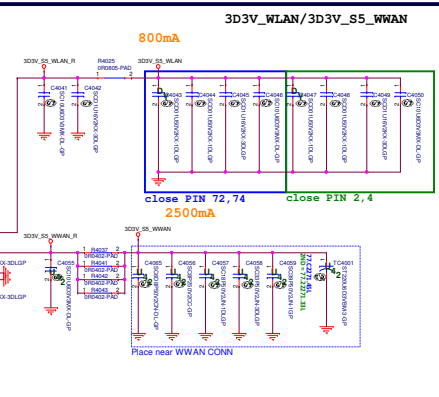
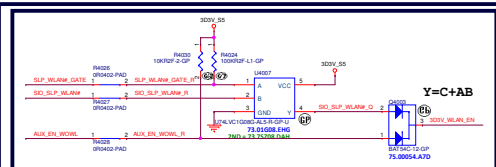
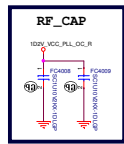
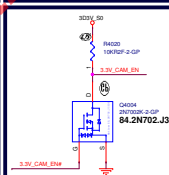
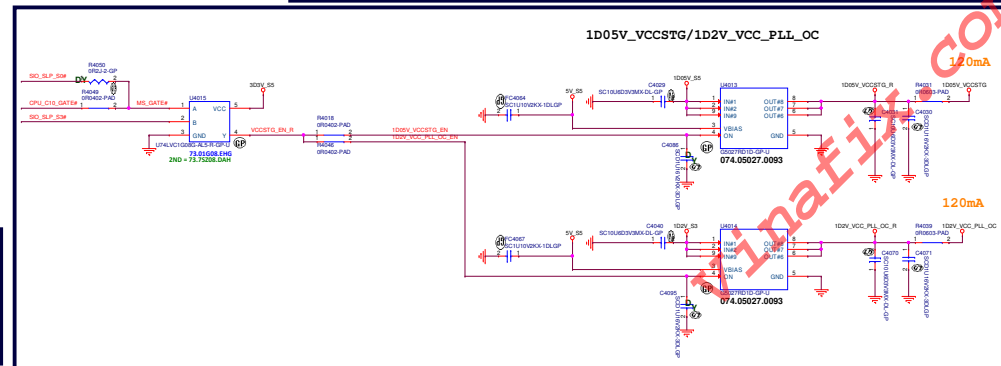
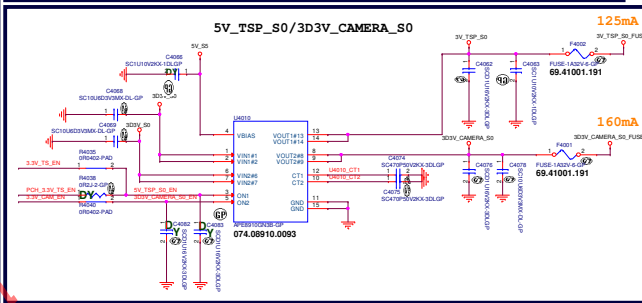
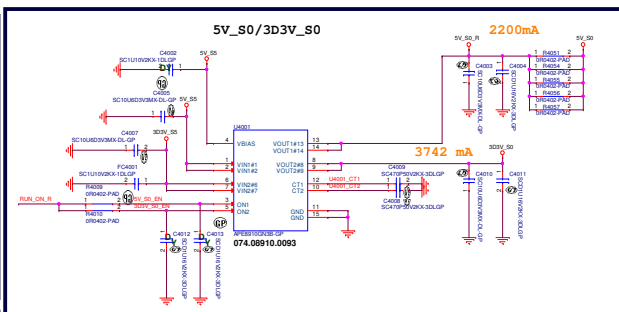
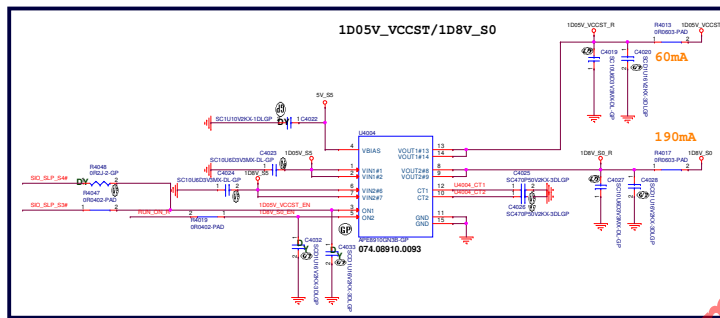
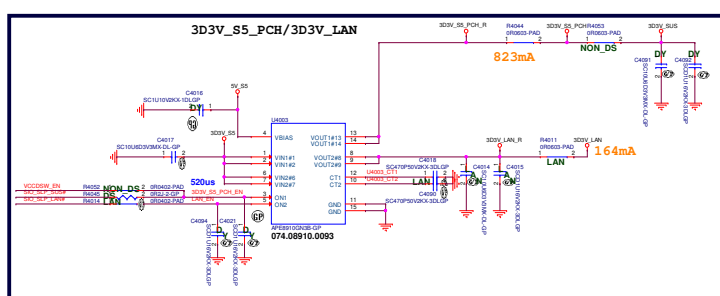
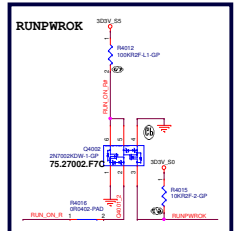
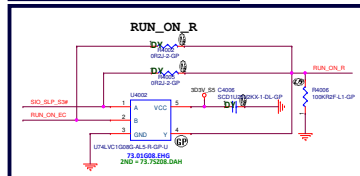
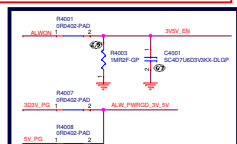
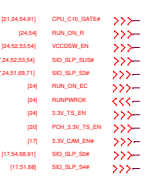
Main Func =

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<Core Design>


			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Sequence (RSVD)</b>					
Size	Document Number				Rev
A4	<b>Bandon / NorthBay 13"</b>				<b>X00</b>
Date: Friday, February 15, 2019		Sheet		39	of 106

[24]	ALWON	>>>—
[45]	3V5V_EN	<<<—
[45]	303V_PG	>>>—
[45]	5V_PG	>>>—
[45]	ALW_PWRIGD_3V_5V	<<<—
[17]	SIO_SLP_LAN#	>>>—
[24]	SLP_WLAN#_GATE	>>>—
[17]	SIO_SLP_WLAN#	>>>—
[45]	AUX_EN_WOW#	>>>—
[24]	3.5V_WWAN_EN	>>>—




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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Sequence (RSVD) (DS3/S0ix)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet    41    of	106

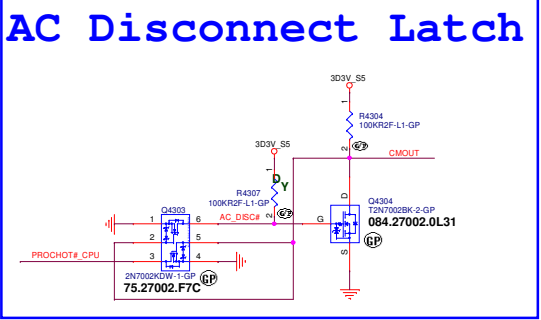
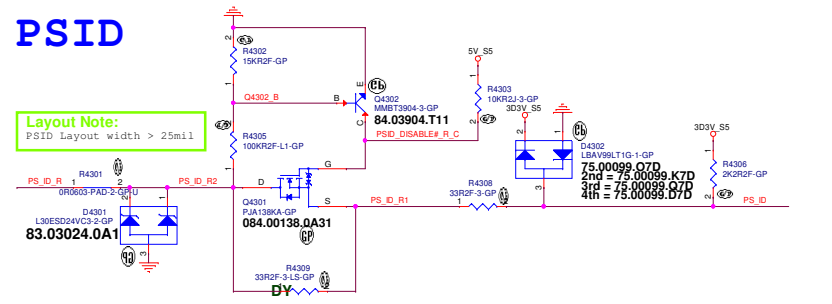
vinafix.com

<Core Design>

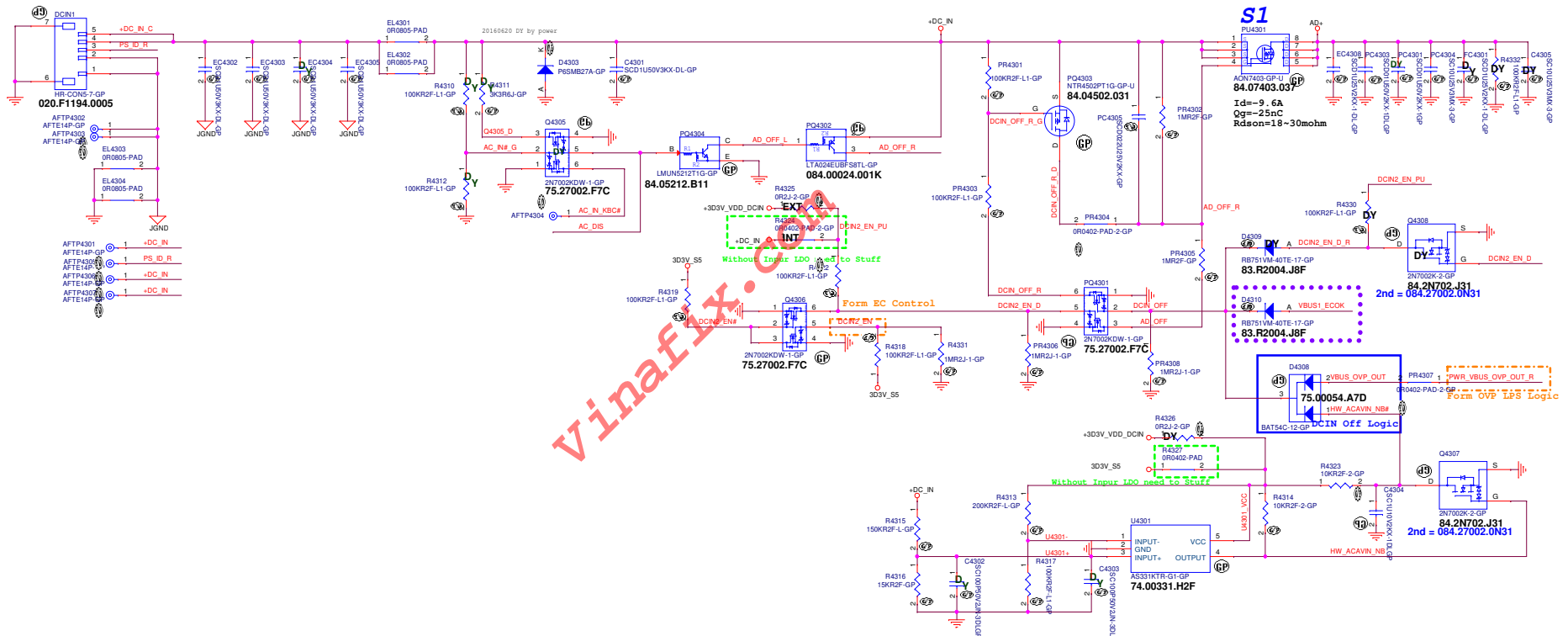
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>INT IO (RSVD)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 42 of	106

Main Func = DCIN & BATT Com

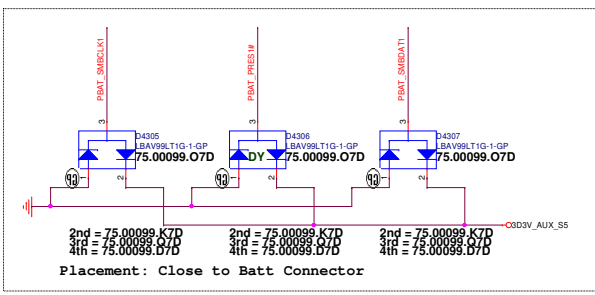
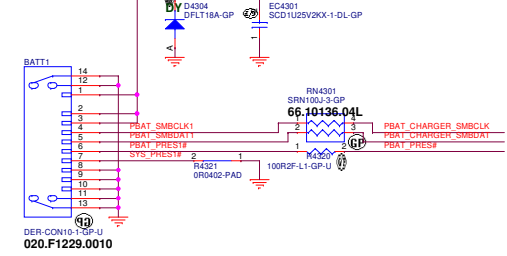
[24] PS\_ID <<< ---  
[3,24,44,4] PROCHOT#\_CPU <<< ---  
[44] CMOUT <<< ---  
[24,44] AC\_DIS >>> ---  
[24] DCN2\_EN >>> ---  
[24,44] PBAT\_CHARGER\_SMBCLK <<< ---  
[24,44] PBAT\_CHARGER\_SMBDAT <<< ---  
[24,44] PBAT\_CHARGER\_SMBEN <<< ---  
[74] PWR\_VBUS\_OVP\_OUT\_R >>> ---  
[24,74] AC\_DIS# <<< ---  
[24,44,74] HW\_ACAVIN\_NB <<< ---  
[24,74] VBUS1\_ECOK >>> ---



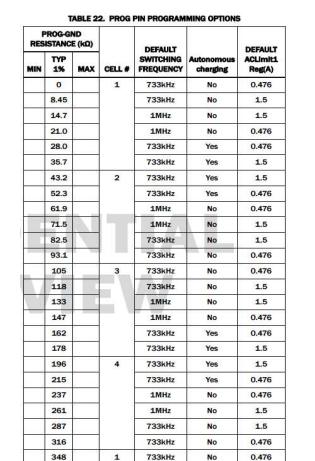
### DC\_IN



### Batt Connector

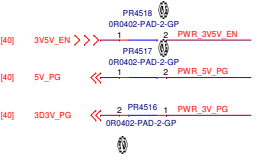


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Main Func = Power_Charger
```

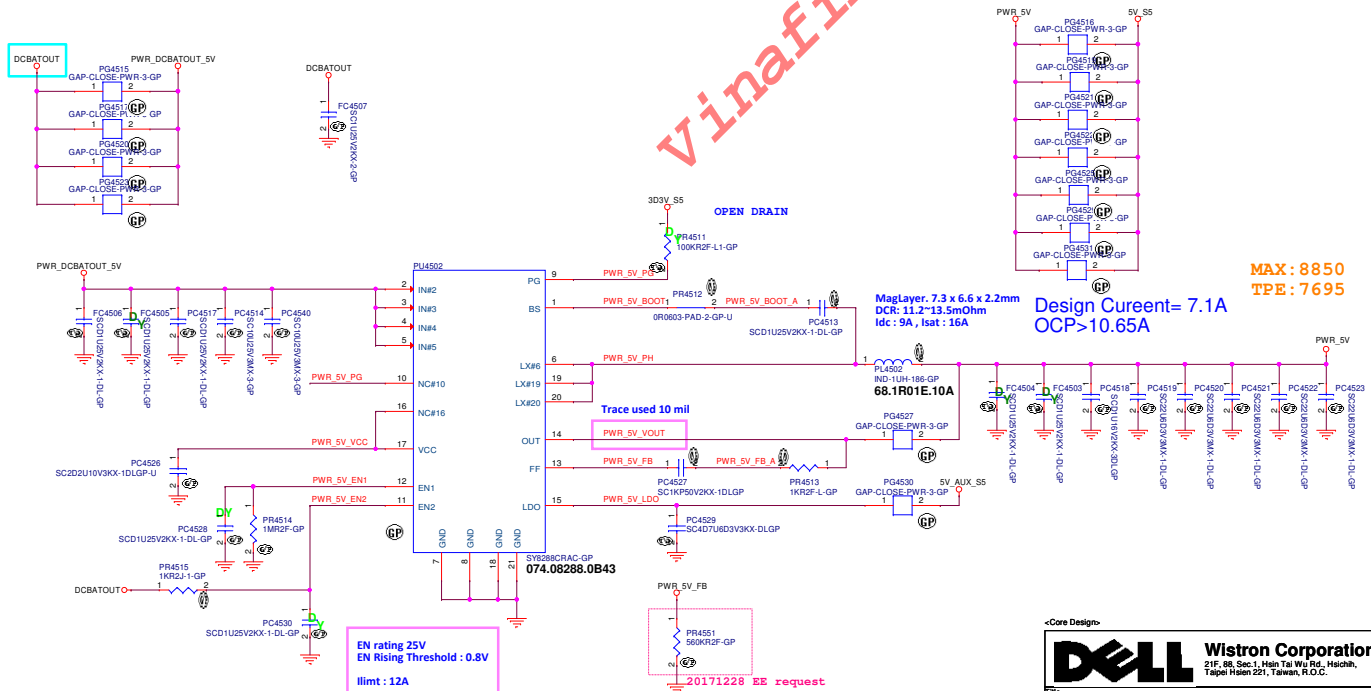
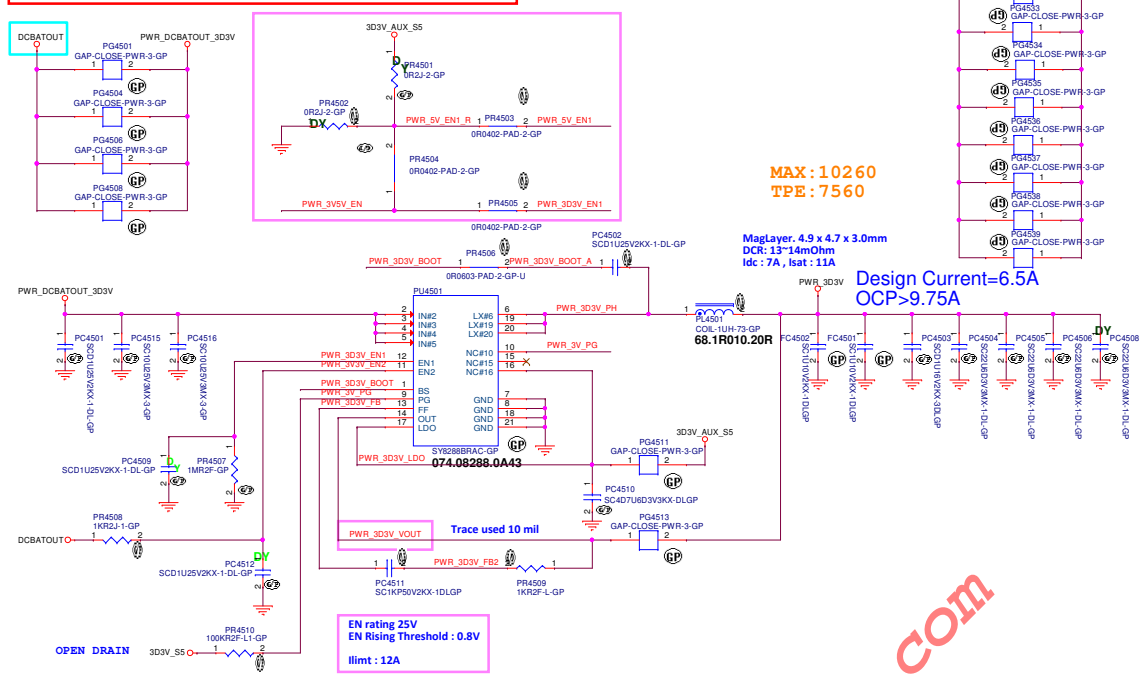




OFFPAGE



Main Func = Power\_System 5V/3D3V



Core Design

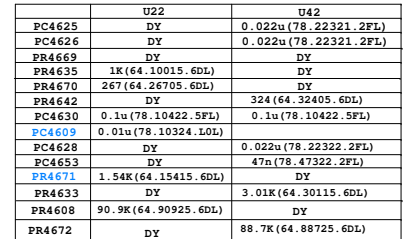
**DELL** Wistron Corporation  
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File: **5V/3D3V**

Size: Document Number  
Custom: **Bandon / NorthBay 13"** Rev: **X00**

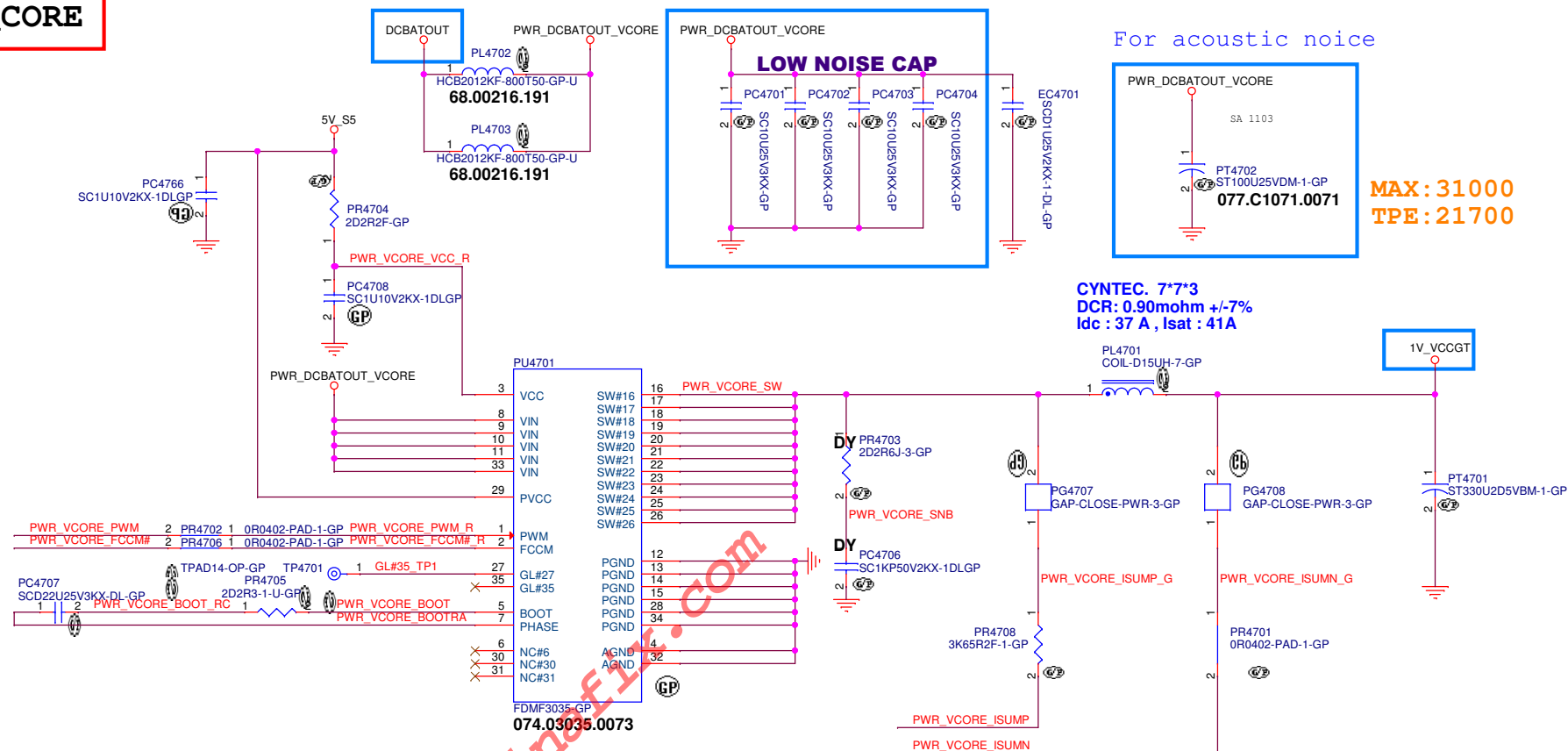
Date: Friday, February 15, 2019 Sheet: 45 of 106

[7]	SVID_CLK_CPU	<<<
[7]	SVID_ALERTA_CPU	<<<
[7]	SVID_DATA_CPU	<<<
[7]	VCCCORE Sense	<<<
[7]	VSSCORE Sense	<<<
[48]	PWR_VCCGT_SUMP	>>>
[48]	PWR_VCCGT_SUMN	>>>
[48]	PWR_VCCGT_SEN1	>>>
[48]	PWR_VCCGT_SEN2	>>>
[8]	VSSGT Sense	<<<
[8]	VCCGT Sense	<<<
[47]	PWR_VCORE_SUMN	>>>
[47]	PWR_VCORE_SUMP	>>>
[50]	PWR_VCCSA_SUMN	>>>
[50]	PWR_VCCSA_SUMP	>>>
[8]	VSSSA Sense	<<<
[8]	VCCSA Sense	<<<
[48]	PWR_VCCGT_FCCM	>>>
[48]	PWR_VCCGT_FWMA	>>>
[48]	PWR_VCCGT_FWMB	>>>
[50]	PWR_VCCSA_FWM	>>>
[50]	PWR_VCCSA_FCM	>>>
[47]	PWR_VCORE_FWM	>>>
[47]	PWR_VCORE_FCM	>>>
[24]	VR_EN	>>>
[3,24,43,44]	PROCHOT#_CPU	<<<
[17]	PCH_PWRKOK	<<<
[24,44]	LSYS_R	<<<



```
Main Func = CPU_CORE
```

```
[46] PWR_VCORE_PWM    >>>—
[46] PWR_VCORE_FCCM#   >>>—
[46] PWR_VCORE_ISUMP    <<<—
[46] PWR_VCORE_ISUMN    <<<—
```



## <Core Design>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**ISL95859C CPU VCORE(2/3)**

Size	
Custom	

Document Number **Banc**

**Bandon / NorthBay 13"**

Rev	X00
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Date: Friday, February 15, 2019

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rv 15 2

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apt

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[46]	PWR_VCCGT_PWMA	>>—
[46]	PWR_VCCGT_FCCM#	>>—
[46]	PWR_VCCGT_ISEN1	<<—
[46]	PWR_VCCGT_ISUMP	<<—
[46]	PWR_VCCGT_ISUMN	<<—
[46]	PWR_VCCGT_ISEN2	<<—
[46]	PWR_VCCGT_PWMB	>>—



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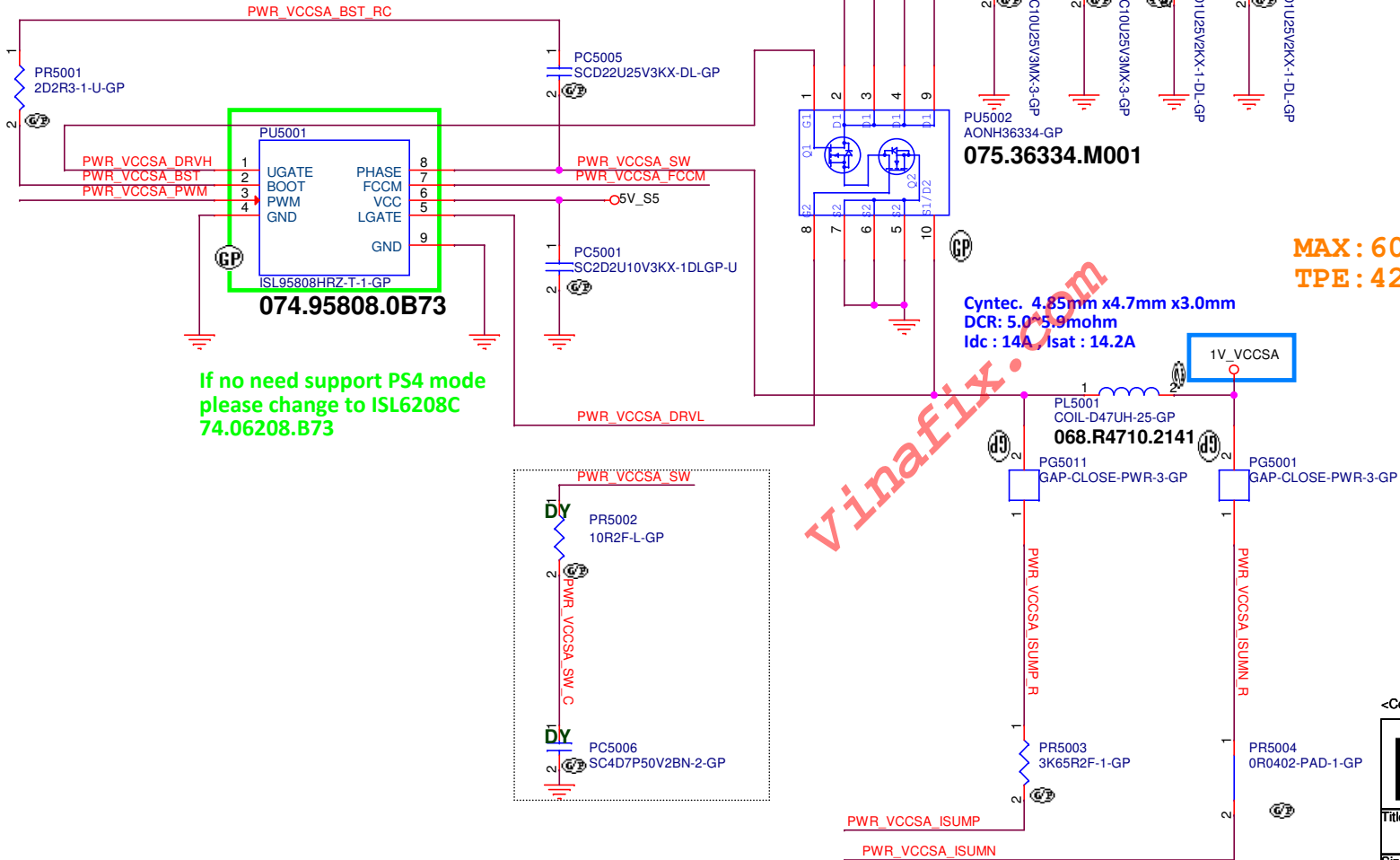
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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>NCP81210MN_CPU_VCCGTUS</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 49 of 106

Main Func = CPU\_VCCSA

[46] PWR\_VCCSA\_PWM >>>—  
[46] PWR\_VCCSA\_ISUMP <<<—  
[46] PWR\_VCCSA\_ISUMN <<<—  
[46] PWR\_VCCSA\_FCCM >>>—



<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>VCCSA</b>	
Size	Document Number		Rev	
Custom	<b>Bandon / NorthBay 13"</b>		<b>X00</b>	
Date:	Friday, February 15, 2019		Sheet	50 of 106



Main Func = Power\_VDDQ/VTT/2D5V/0D6V

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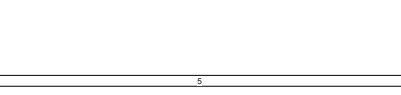
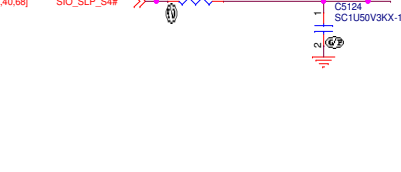
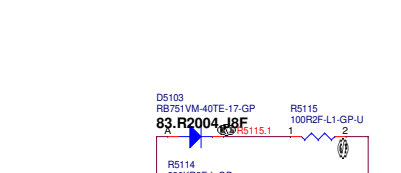
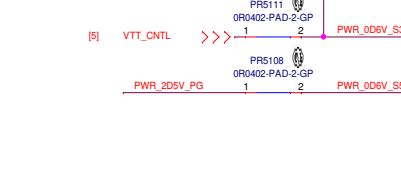
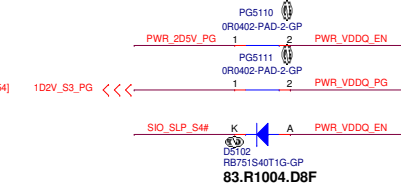
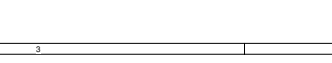
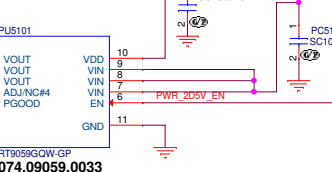
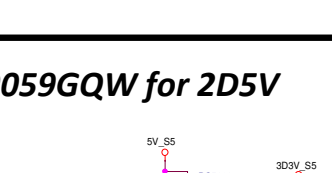
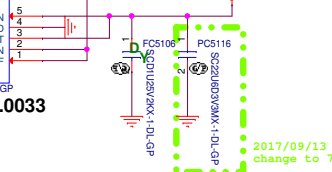
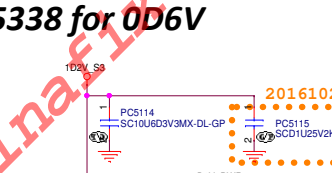
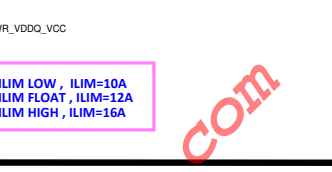
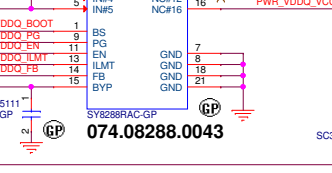
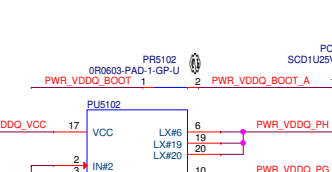
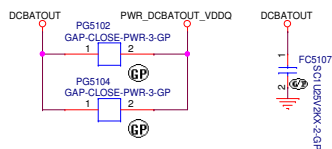
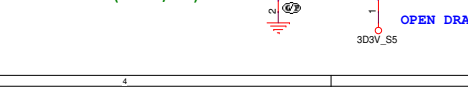
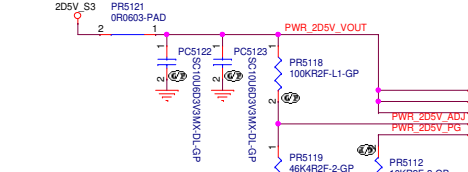
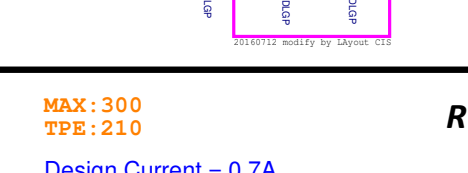
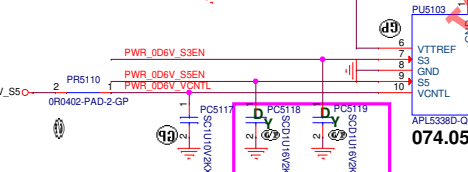
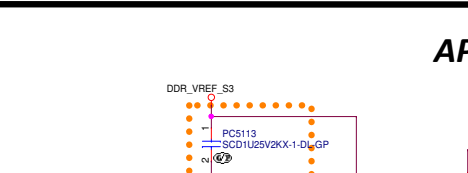
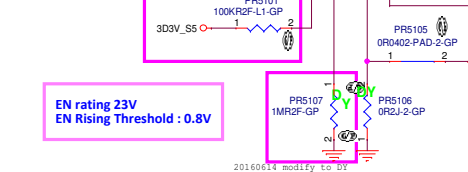
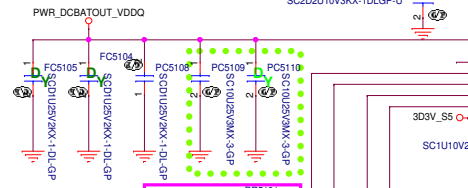


Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

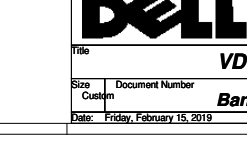
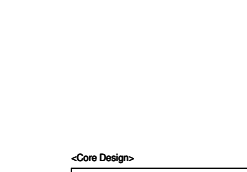
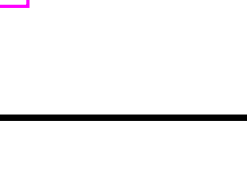
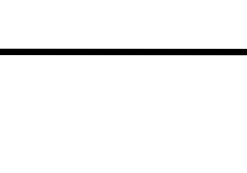
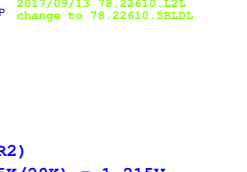
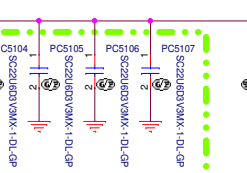
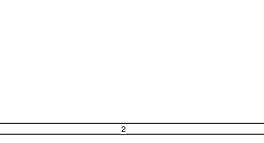
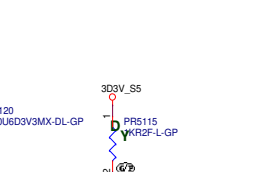
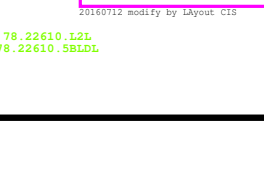
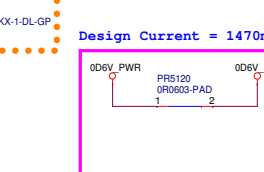
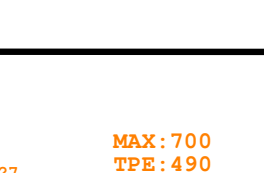
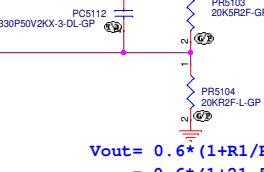
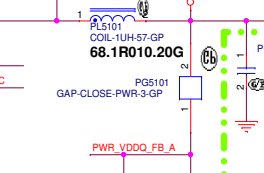


SY8288RAC for 1D2V

MAX:13300  
TPE:9310

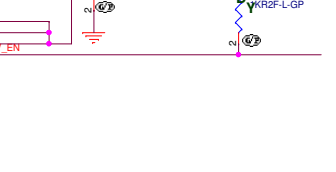
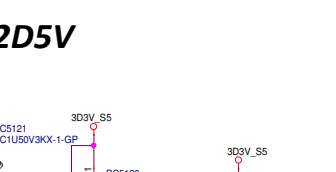
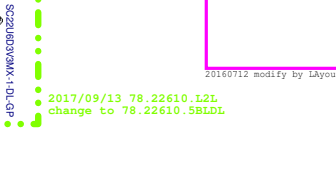
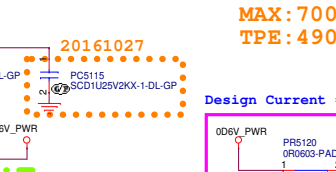
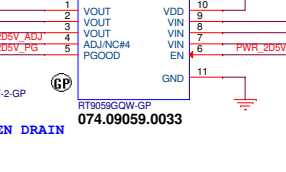
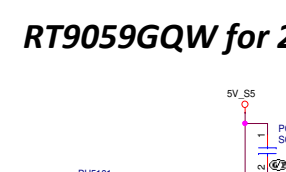
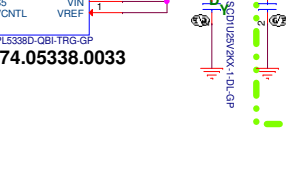
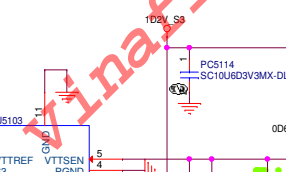
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DCR: 9\*10mOhm  
Idc:9A, Isat: 11A

Design Current=7.868A  
Icc(max)=11.24A  
OCP>12A



APL5338 for 0D6V

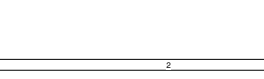
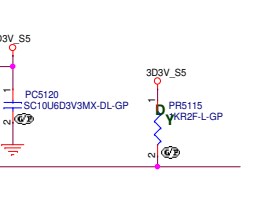
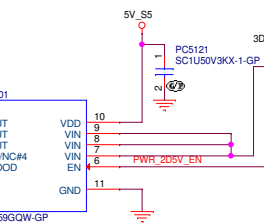
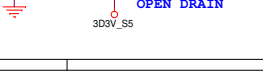
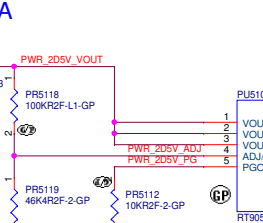
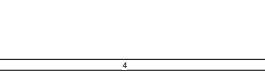
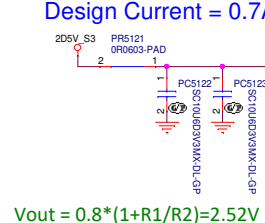
MAX:700  
TPE:490



RT9059GQW for 2D5V

MAX:300  
TPE:210

Design Current = 0.7A



<Core Design>

**DELL** Wistron Corporation  
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipexi, Taiwan, R.O.C.

Title **VDDQ/VTT**

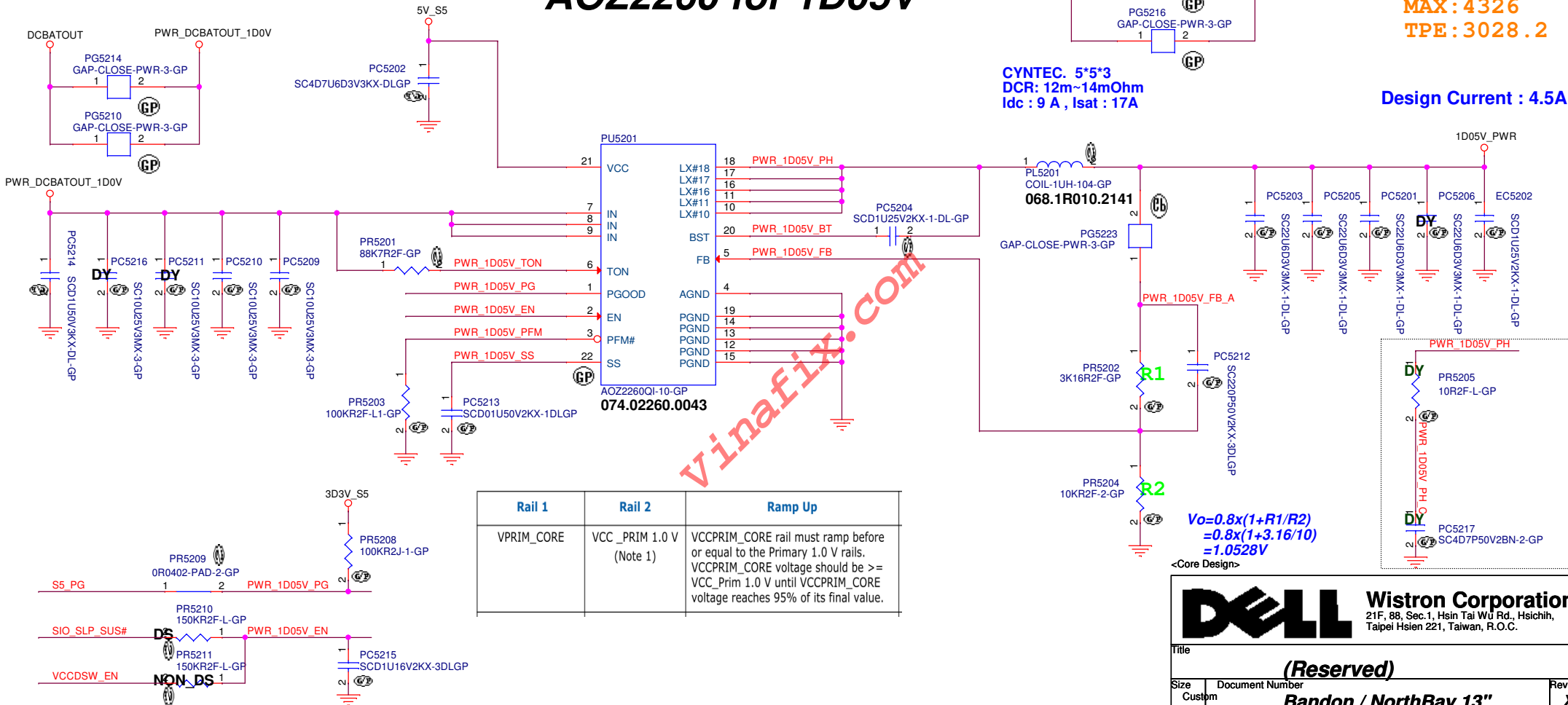
Size Custom Document Number **Bandon / NorthBay 13"** Rev **X00**

Date: Friday, February 15, 2019 Sheet 51 of 106

SSID = PWR.Plane.Regulator\_1D05V

[24,53,54] S5\_PG <<<—  
[17,24,40,53,54] SIO\_SLP\_SUS# >>>—  
[24,40,53,54] VCCDSW\_EN >>>—

## AOZ2260 for 1D05V



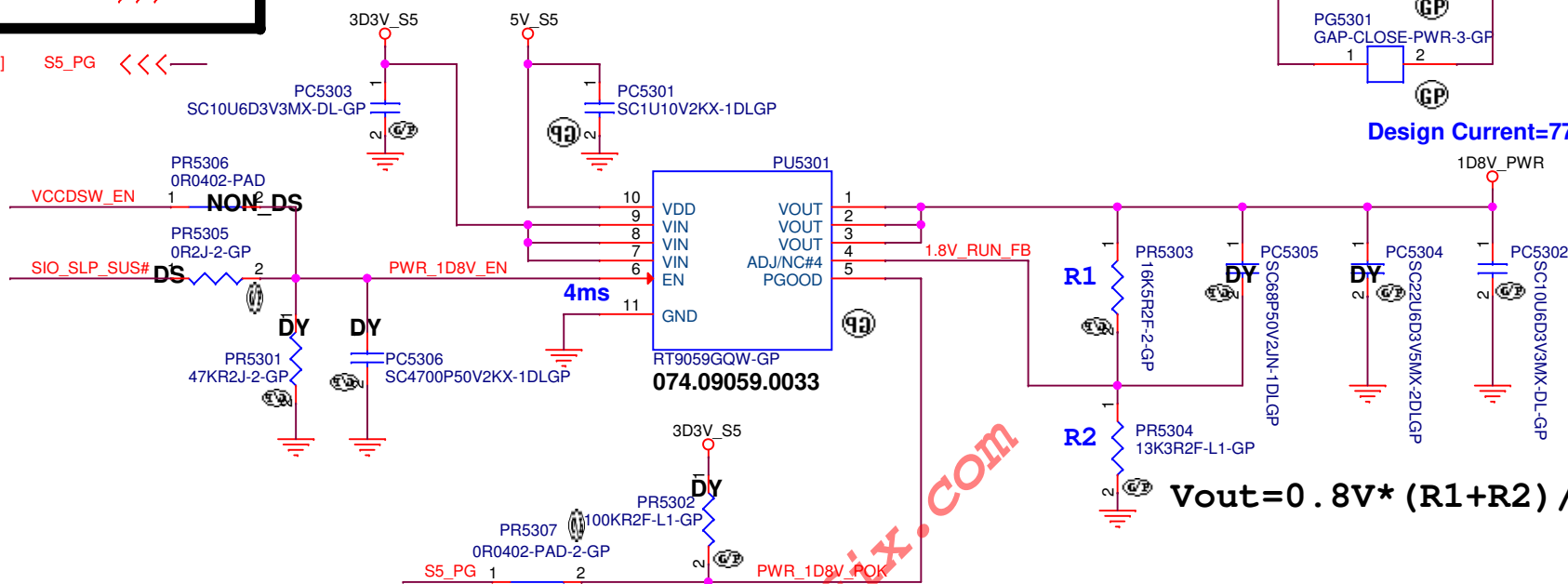
Main Func = 1D8V

## APL5934 for 1D8V\_S5

MAX: 917  
TPE: 641.9

Design Current=770mA

$$V_{out} = 0.8V * (R1 + R2) / R2$$



<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size  
A4

Document Number

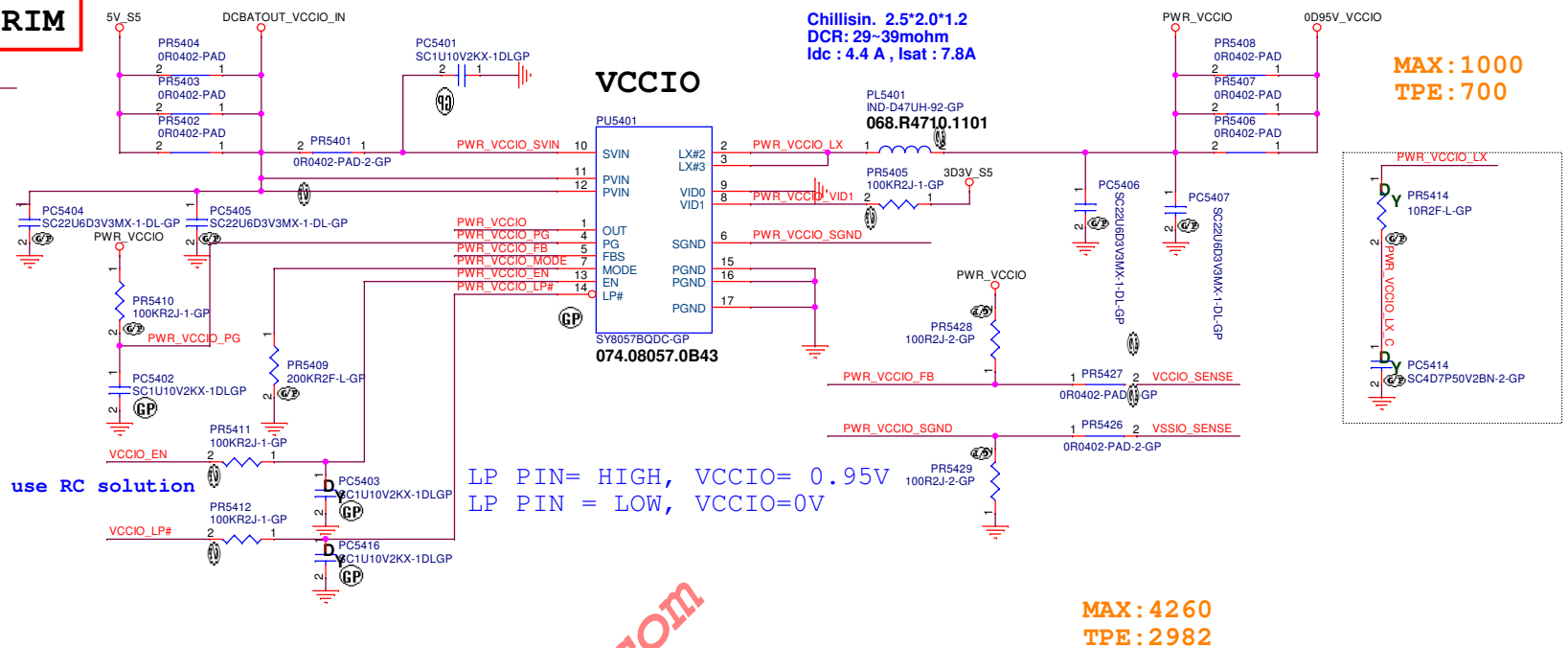
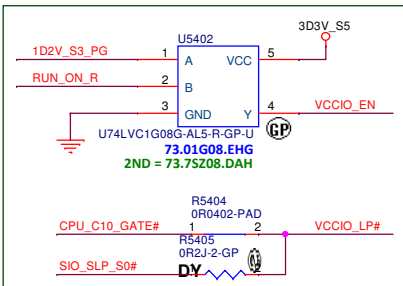
Bandon / NorthBay 13"

Rev  
X00

Date: Friday, February 15, 2019

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[8]	VCCIO_SENSE	>>>	_____	
[8]	VSSIO_SENSE	>>>	_____	[24,52,53] SS_PG <<<_____
[24,40]	RUN_ON_R	>>>	_____	
[51]	1D2V_S3_PG	>>>	_____	
[21,24,40,91]	CPU_C10_GATE#	>>>	_____	
[17,40,68,91]	SIO_SLP_S0#	>>>	_____	
[24,40,52,53]	VCCDSW_EN	>>>	_____	
[17,24,40,52,53]	SIO_SLP_SUS#	>>>	_____	
[22]	PRIMCORE_G0	>>>	_____	
[22]	PRIMCORE_G1	>>>	_____	
[20]	PRIM_CORE_OPT_DI#	>>>	_____	



0V2KX-1DLGP

1

PR5402

PRIMCORE\_SVIN 10 SVIN

11 LX#2

12 LX#3

PVIN VID#0

PVIN VID#1

1 OUT

2 PG

3 FBS

4 PRIMCORE\_MODE

5 MODE

6 PRIMCORE\_EN

7 EN

8 PRIMCORE\_LPF

14 LP#

SGND

PGND

PGND

PGND

SY8057CQDC-CP

074.08057.0C43

CYNTCE. 4\*4\*2

DCR: 24~27mohm

I<sub>dc</sub> : 4.5A, I<sub>sat</sub> : 7A

PL5402

IND-1UH-129-GP-U

68.1R010.20D

PWR\_PRIMCORE\_LX 1

PR5430

0R2J-2-GP

PWR\_PRIMCORE\_G0

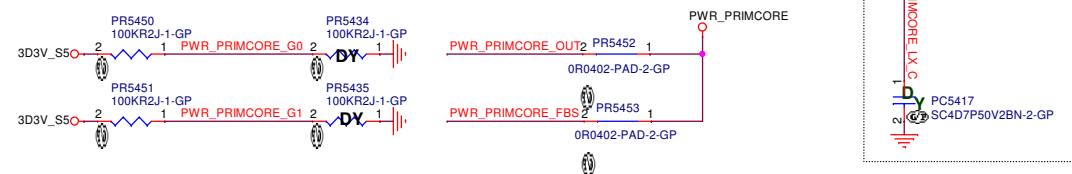
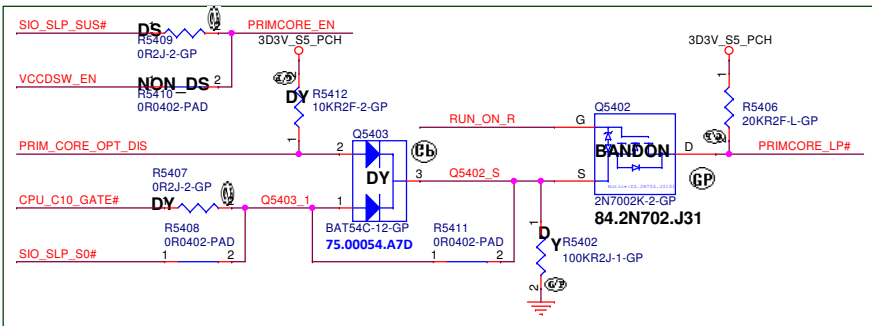
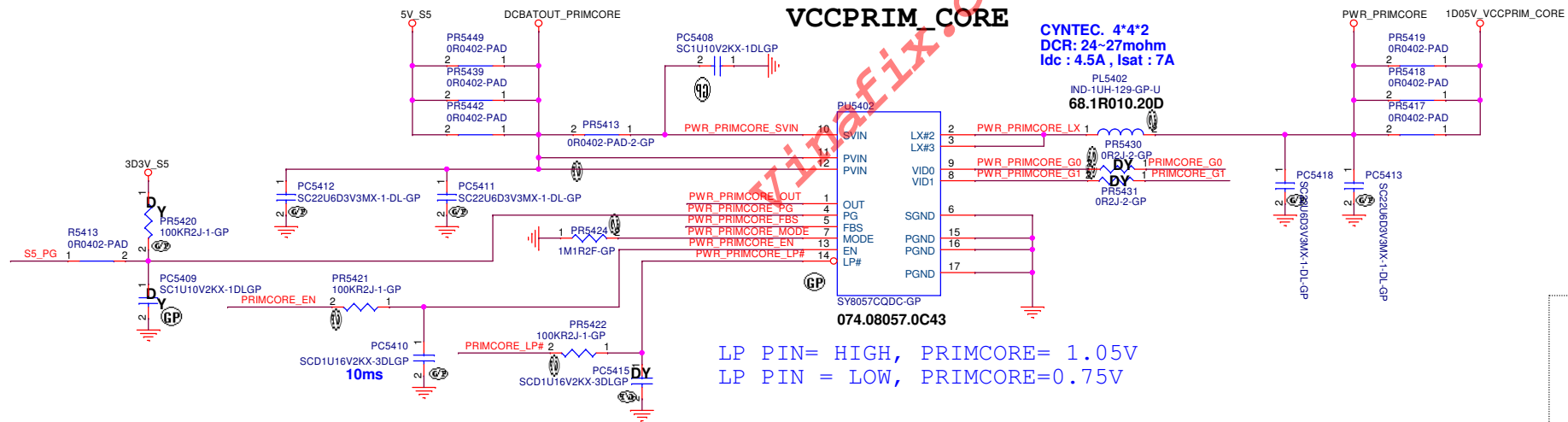
PWR\_PRIMCORE\_G1

PR5431

0R2J-2-GP

LP PIN= HIGH, PRIMCORE= 1.05V

LP PIN= LOW, PRIMCORE=0.75V



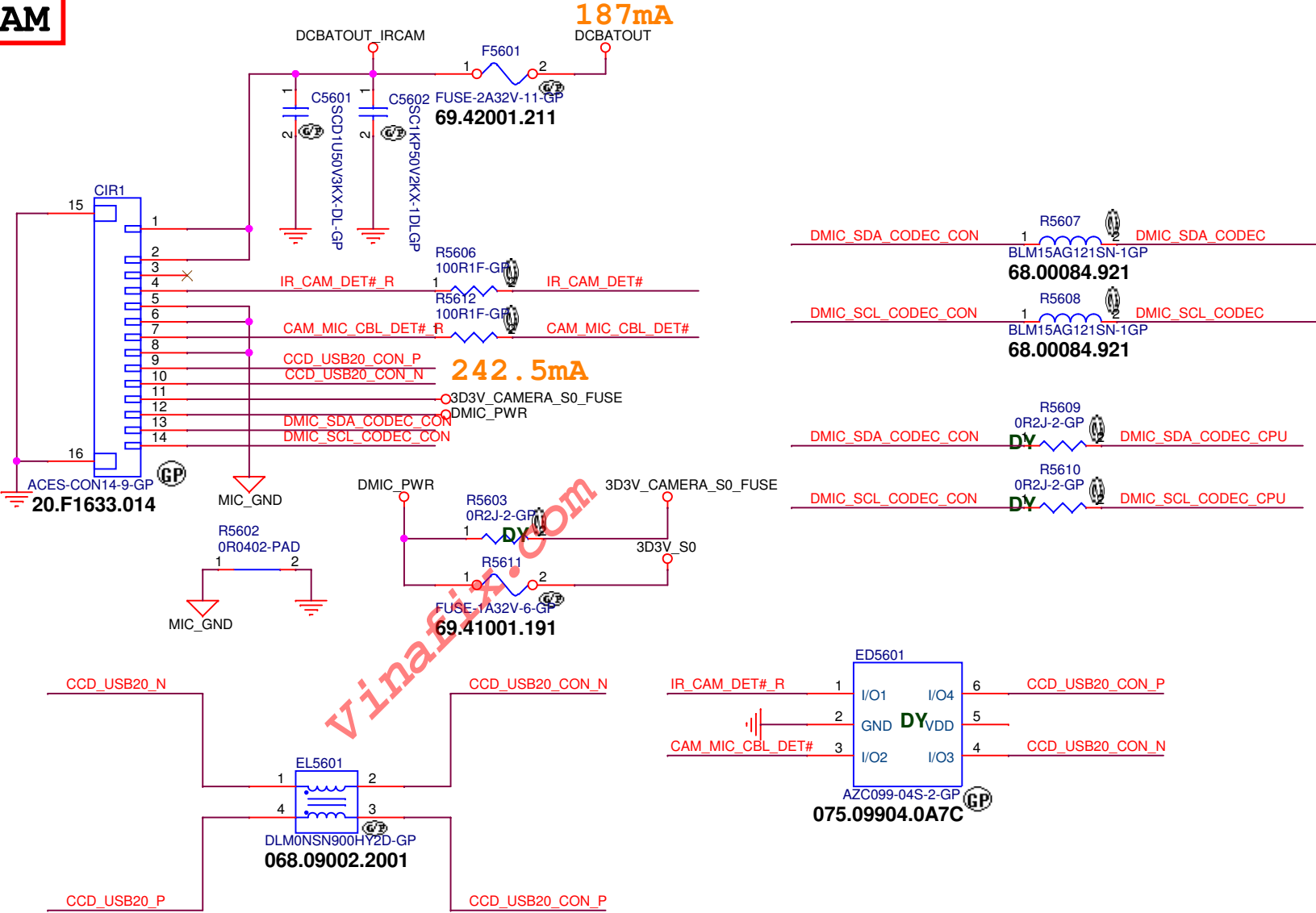
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<b>Title</b>			
<b>&lt;Title&gt;</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
<b>A3</b>	<b>Bandon / NorthBay 13"</b>		<b>X00</b>
<b>Date:</b>	<b>Friday, February 15, 2019</b>	<b>Sheet</b>	<b>54 of 106</b>



Main Func = IR CAM

CAMERA

[16]	CCD_USB20_N	<<<<
[16]	CCD_USB20_P	<<<<
[27]	DMIC_SDA_CODEC	>>>>
[27]	DMIC_SCL_CODEC	>>>>
[20]	IR_CAM_DET#	<<<<
[19]	CAM_MIC_CBL_DET#	<<<<
[19]	DMIC_SDA_CODEC_CPU	>>>>
[19]	DMIC_SCL_CODEC_CPU	>>>>

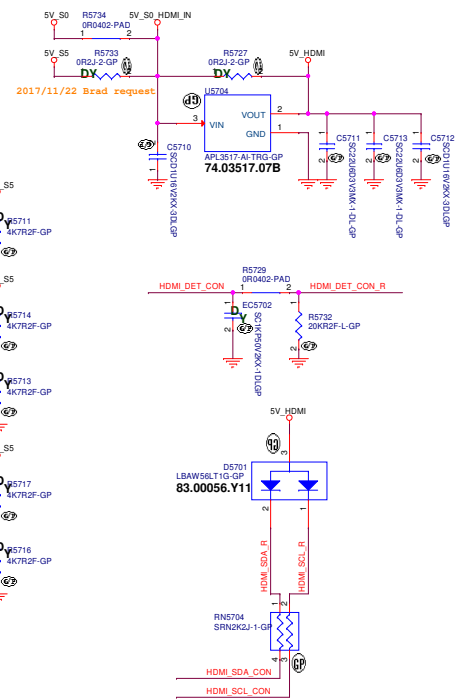
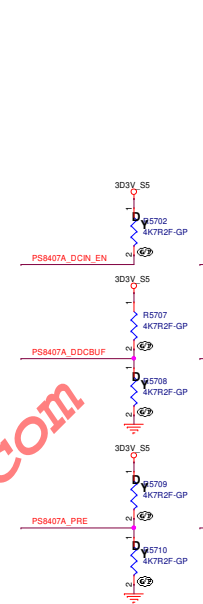
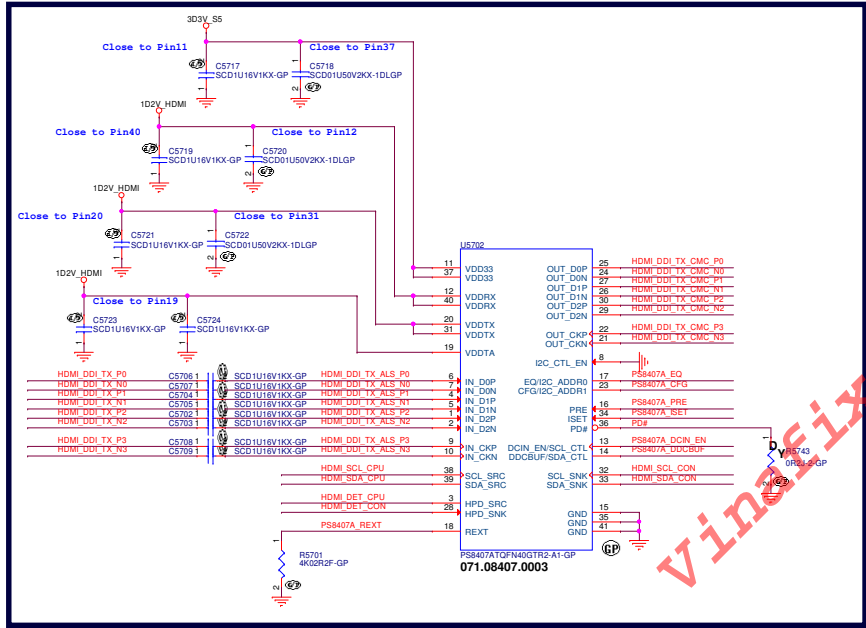
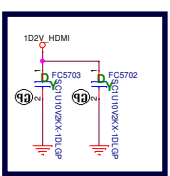
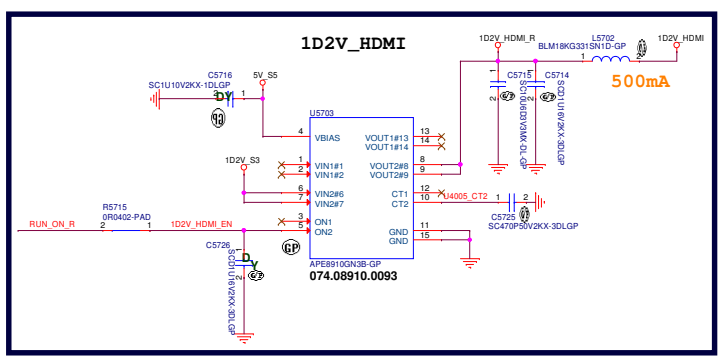
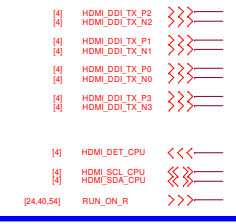


<Core Design>

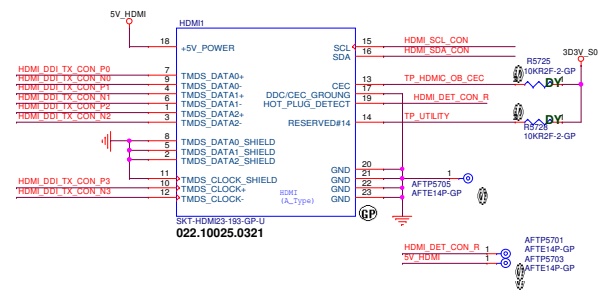
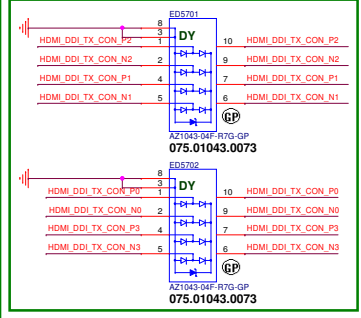
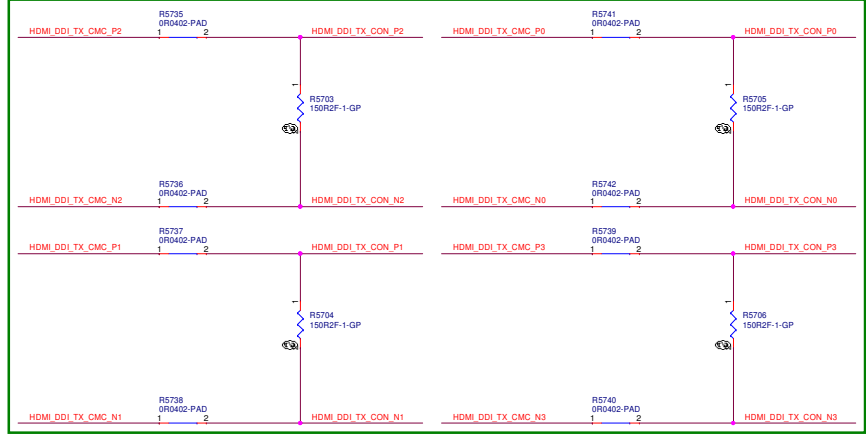
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Display (LCD/Inverter)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 56	of 106



Main Func = HDMI




HDMI CONNECTOR




vinafix.com

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Display (RSVD) DP</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 58 of	106


vinafix.com

<Core Design>

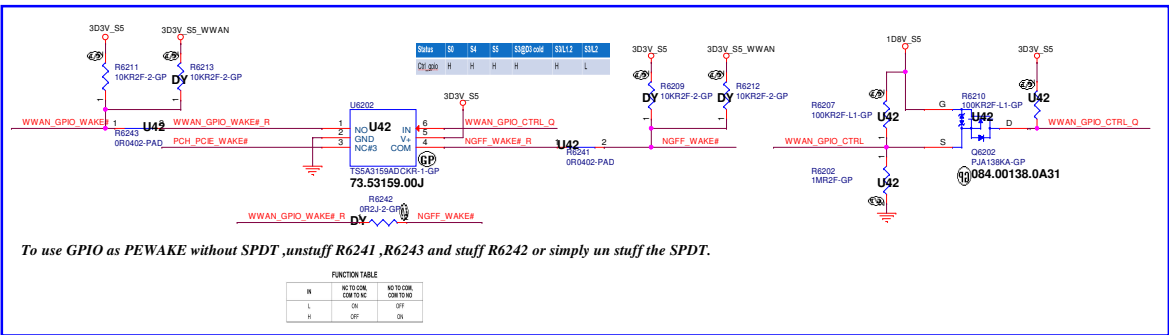
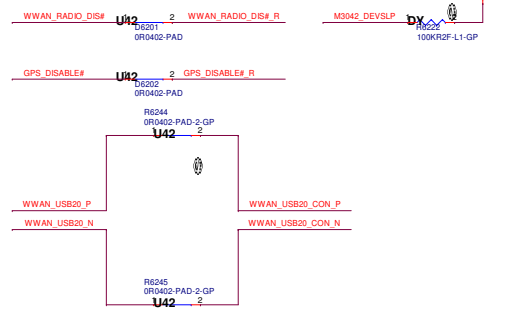
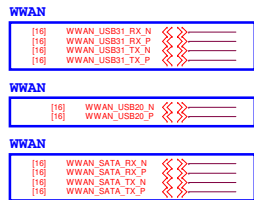
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Display (RSVD) DVI</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 59 of	106

vinafix.com

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>INT IO (RSVD)(HDD)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 60 of 106	

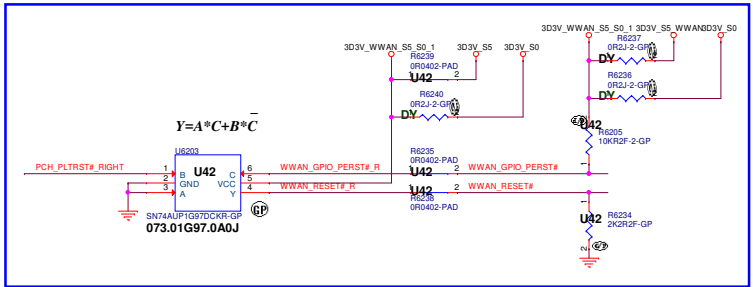


$$NGFF(WWAN/SSD)$$


*To use GPIO as PEWAKE without SPDT ,unstuff R6241 ,R6243 and stuff R6242 or simply un stuff the SPDT.*

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

54	PCWATCHDOG	O	L	<p>Assured to enable up system and disable PCIE link V1.2 to V2.8, depending on system</p> <p>Whether supports wake up functionality depends on the upper-layer control and should not extend pull-up on platform</p>	CMOS 1.5V
55	PERST#	I	T	<p>Assured to reset module PCIe interface before it module went into core dump, it will reset whole</p>	CMOS 1.5V



STATE#	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M0042_POIER_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

The M.2 module configuration as the following table:

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	GND	GND	NC	WWAN-USB3.1, PCIe Gen1	0

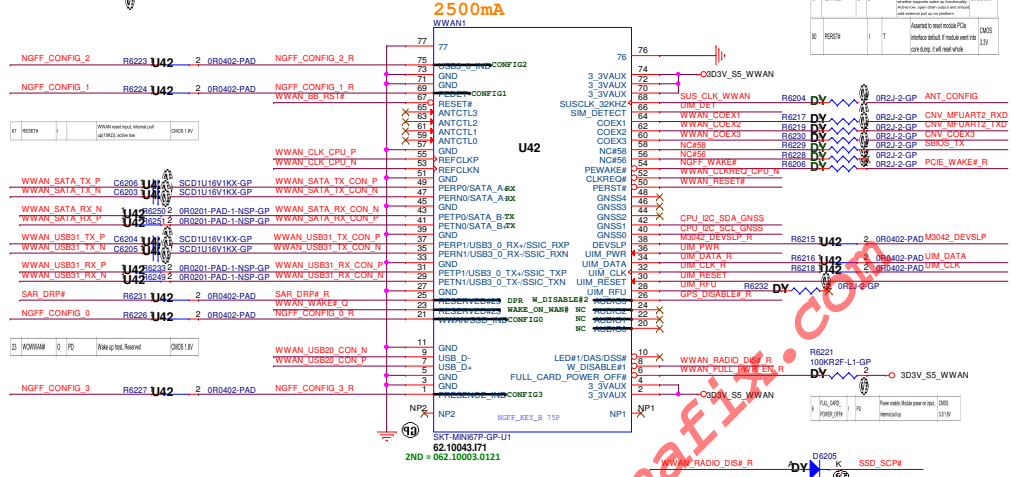
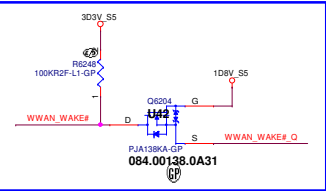
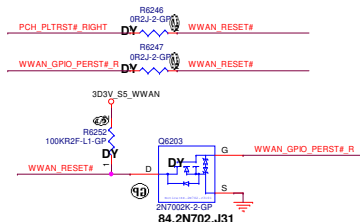


Figure 3-5 Timing Control for Start-up

Index	Minimum	Typical	Notes
t <sub>pr</sub>	-	-	+3.3V power supply rises time. If power supply always ready, there is no t <sub>pr</sub>
t <sub>on1</sub>	10ms	30ms	If the RESET# has a residual voltage, then 30ms is necessary
t <sub>on2</sub>	10ms	30ms	PERST# should de-asserted after FULL_CARD_POWER_OFF#

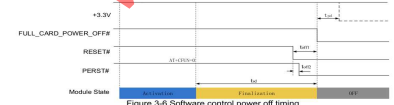
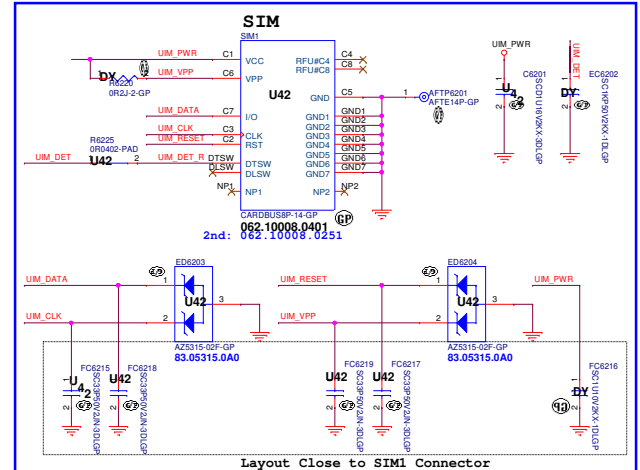


Figure 3-6 Software control power off timing

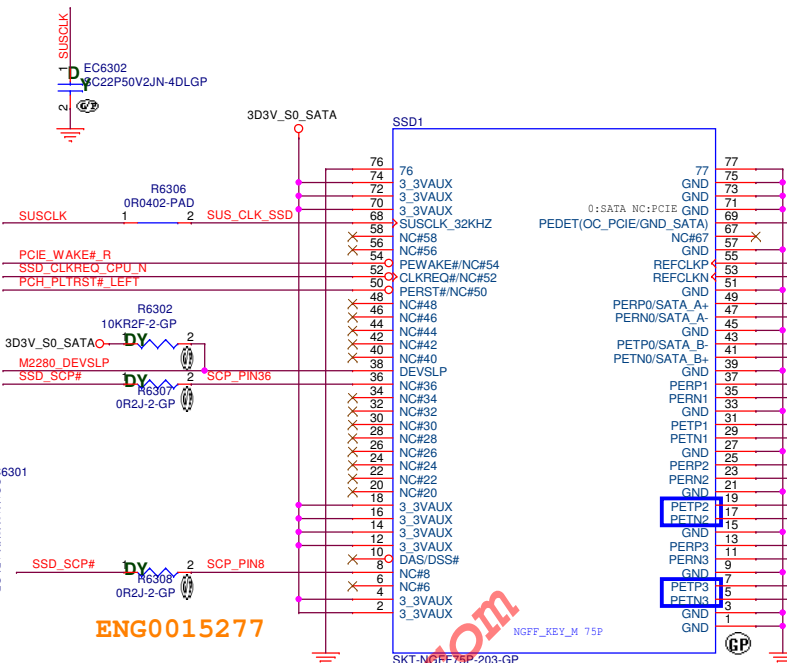
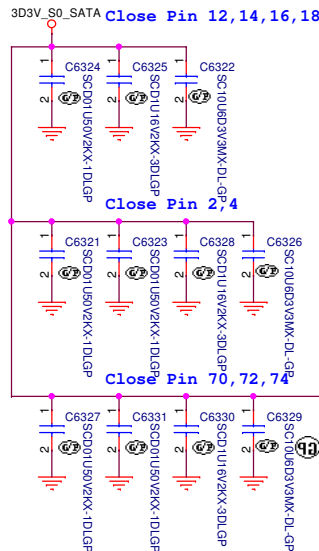
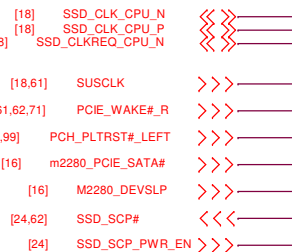
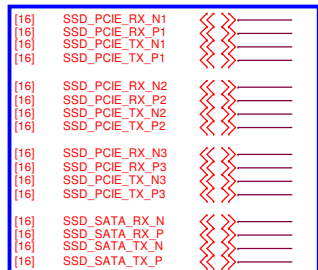
Index	Minimum	Typical	Maxim	Notes
t <sub>pd</sub>	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, there is no t <sub>pd</sub>
t <sub>off1</sub>	10ms	30ms	-	RESET# should asserted before FULL_CARD_POWER_OFF#
t <sub>off2</sub>	0ms	30ms	t <sub>off1</sub>	PERST# should asserted after RESET#



### Layout Close to SIM1 Connector

# Main Func = m.2 SSD

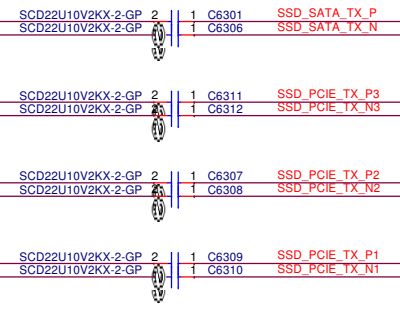
## SSD



PEDET	0	Host I/F Indication; To be grounded for SATA, No Connect for PCIe	OV/NC
L		SATA	
H		PCIe	

SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF	None	None

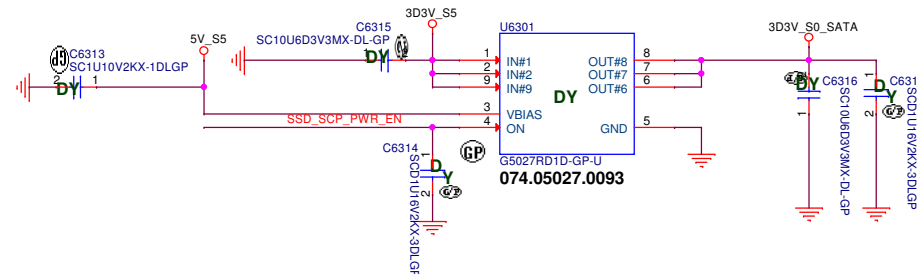
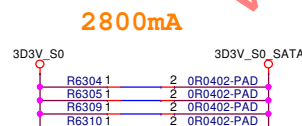


74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
44	N/C	GND	45
42	N/C	PERp0/SATA-B-	43
40	N/C	PERn0/SATA-B+	41
38	DEVSLP (O)	GND	39
36	N/C	PETp1	37
34	N/C	PETn1	35
32	N/C	GND	33
30	N/C	PERp1	31
28	N/C	PERn1	29
26	N/C	GND	27
24	N/C	PETp2	25
22	N/C	PETn2	23
20	N/C	GND	21
18	3.3V	PERp2	17
16	3.3V	PERn2	15
14	3.3V	GND	13
12	3.3V	PETp3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	PETn3	9
8	N/C	GND	7
6	N/C	PERp3	5
4	3.3V	PERn3	3
2	3.3V	GND	1

## 6.5.4.6

## PCH PCI Express\* Controller Lane Reversal

For each PCH PCIe\* Controller we support end-to-end lane reversal across the four lanes mapped to a controller for the following two motherboard PCIe\* configurations



<Core Design>



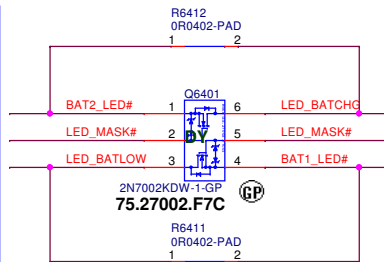
INT IO (SSD M.2/ eMMC)

Size A3 Document Number Bandon / NorthBay 13" Rev X00

Date: Friday, February 15, 2019 Sheet 63 of 106

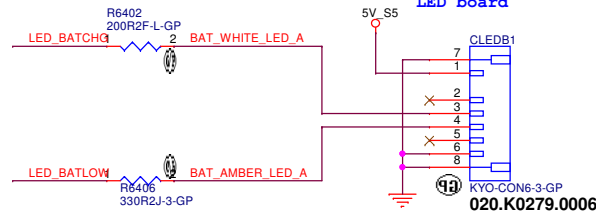
# Main Func = LED/HALL/Button

[24] BAT2\_LED# >>>  
 [24] BAT1\_LED# >>>  
 [24,32] LED\_MASK# >>>  
 [24,66,68] KBC\_PWRBTN# <<<  
 [24,55,67] LID\_CL\_SIO#\_R <<<  
 [24,67] LID\_CL\_SIO\_TAB#\_R >>>  
 [24] BREATH\_LED# <<<  
 [24,92] FPR\_DET# >>>  
 [24] M\_BIST >>>  
 [24,44] ACAV\_IN >>>  
 [17,24,99] RSMRST#\_KBC >>>

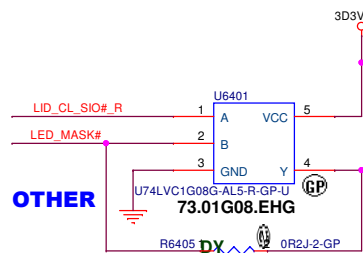
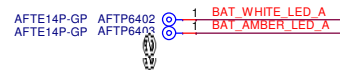


Stealth mode

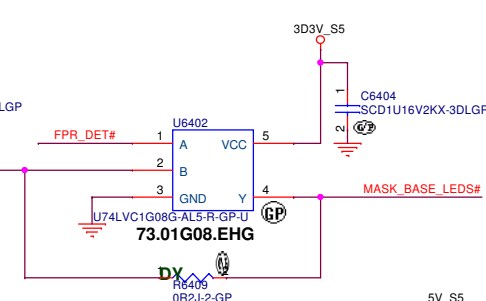
## Battery LED2(White LED) LOW acted from KBC GPIO



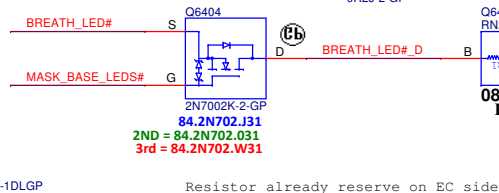
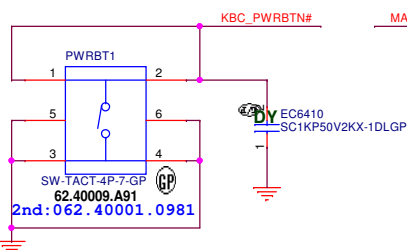
## Battery LED1(Orange LED) LOW acted from KBC GPIO



POWERBT

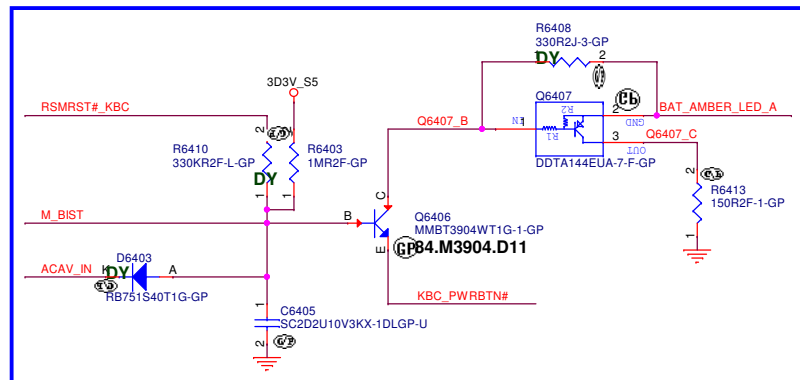


## POWER BUTTON



Power LED  
LOW acted from KBC GPIO

## M-BIST



<Core Design>



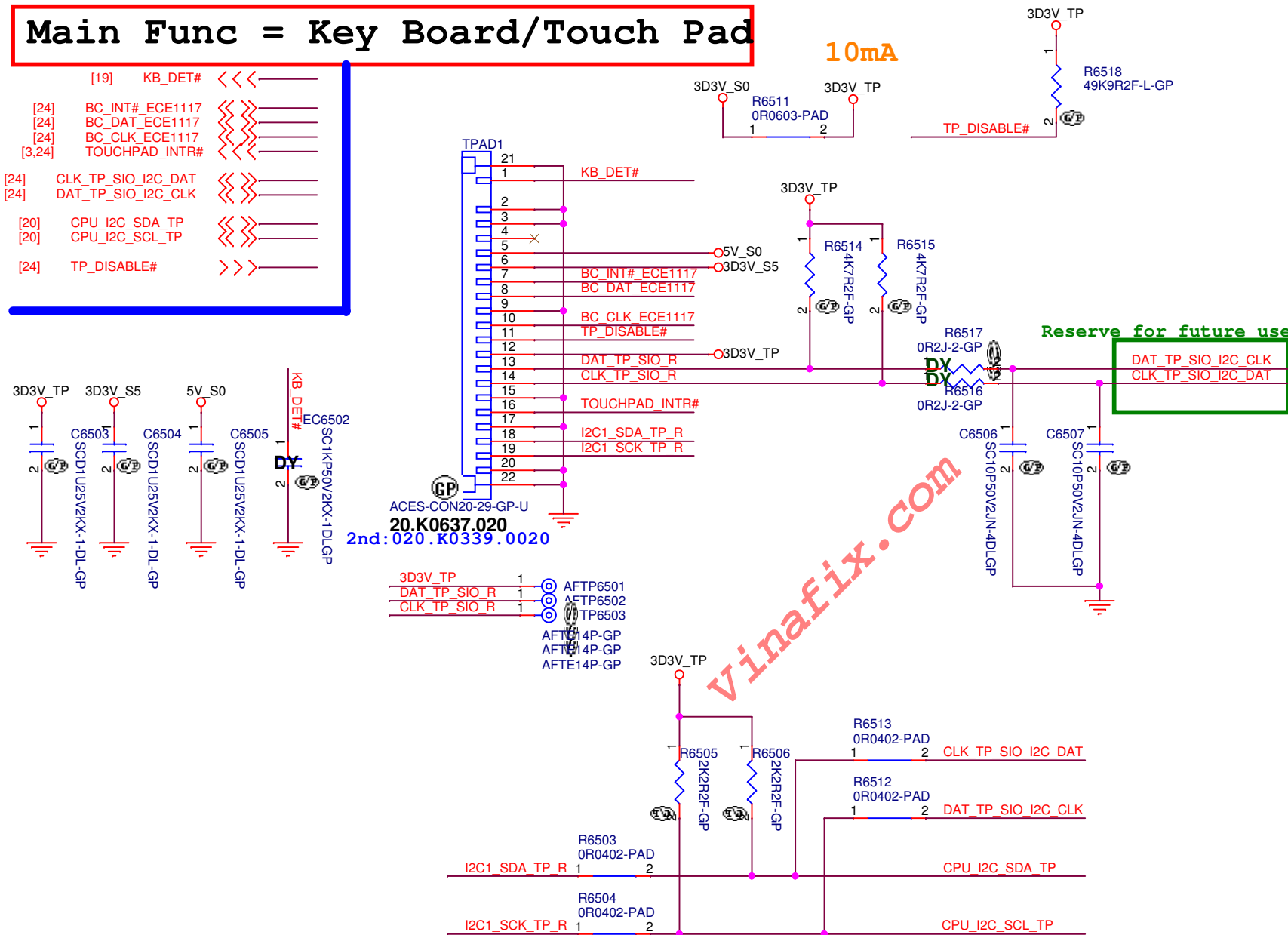
**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title <b>LED / Button / Power Button</b>		
Size Custom	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
Date: Friday, February 15, 2019	Sheet 64	of 106



# Main Func = Key Board/Touch Pad

[19]	KB_DET#	<<<
[24]	BC_INT#_ECE1117	<<<
[24]	BC_DAT#_ECE1117	<<<
[24]	BC_CLK#_ECE1117	<<<
[3,24]	TOUCHPAD_INTR#	<<<
[24]	CLK_TP_SIO_I2C_DAT	<<<
[24]	DAT_TP_SIO_I2C_CLK	<<<
[20]	CPU_I2C_SDA_TP	<<<
[20]	CPU_I2C_SCL_TP	<<<
[24]	TP_DISABLE#	>>>



20.K0637.020  
2nd:020.K0339.0020

<Core Design>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**INT IO (KB/TP)**

Size  
A4

Document Number

**Bandon / NorthBay 13"**

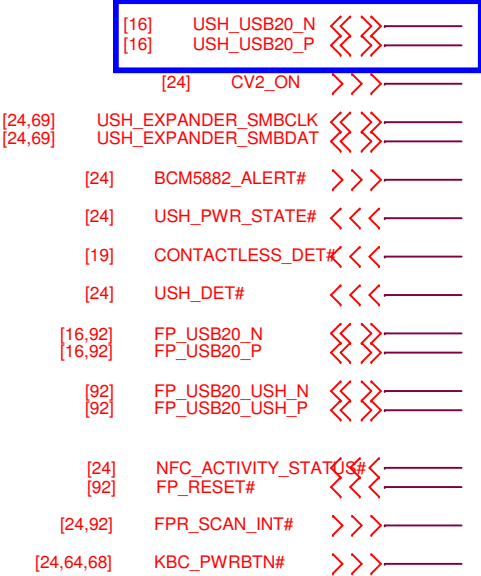
Rev  
**X00**

Date: Friday, February 15, 2019

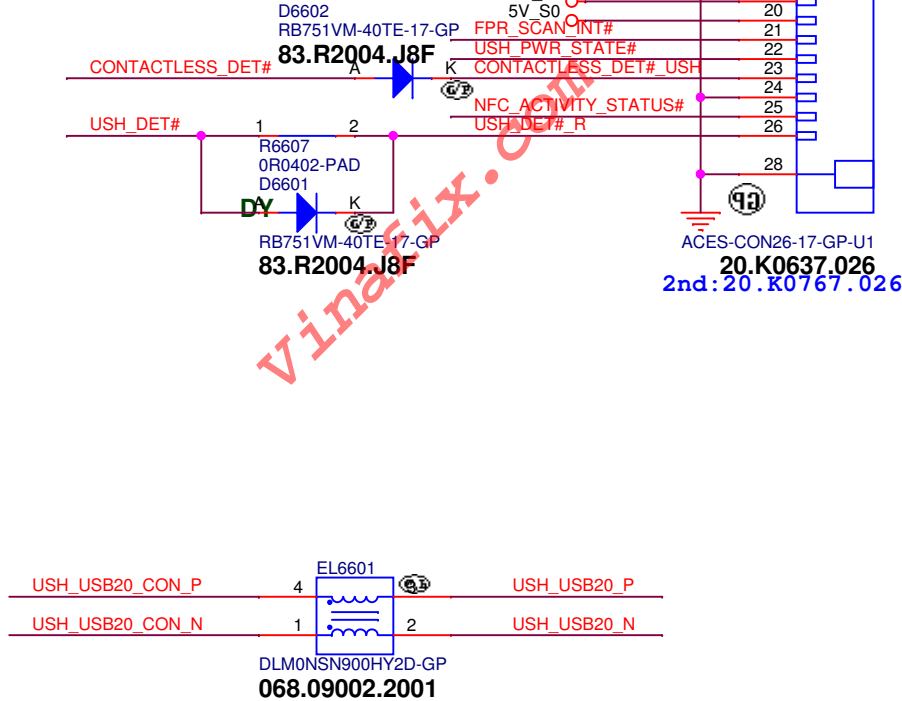
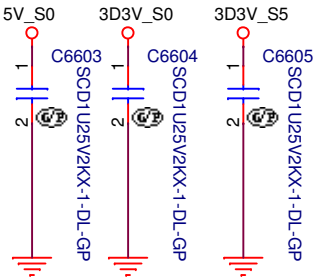
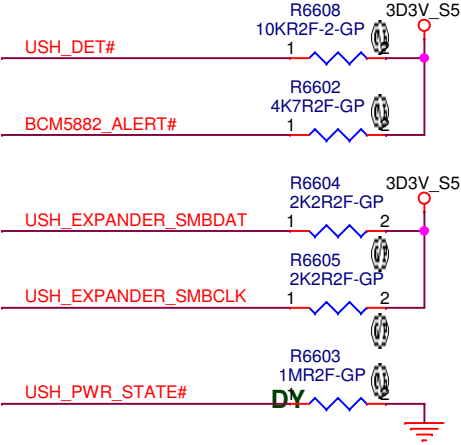
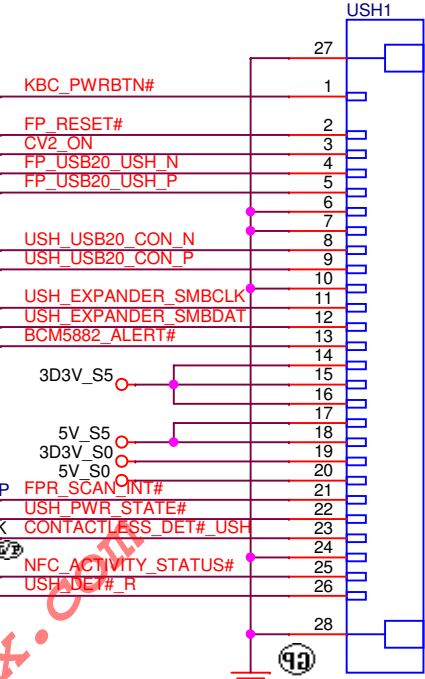
Sheet 65 of 106

Main Func = USH BD

USH



CV3 module	
pin assignment -proposal 2	
NC	
NC	
CV2_ON	
USB20_N from FPR	
USB20_P from FPR	
GND	
GND	
USB20_N to PCH	
USB20_P to PCH	
GND	
USH_EXPANDER_SMBCLK	
USH_EXPANDER_SMBDAT	
BCM5882_ALERT#	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_ALW	
NC	
+5V_ALW	
+3.3V_RUN	
+5V_RUN	
USH_RST#	
USH_PWR_STATE#	
CONTACTLESS_DET#	
GND	
GND	
USH_DET#	



<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **IO Board Conn (USH)**

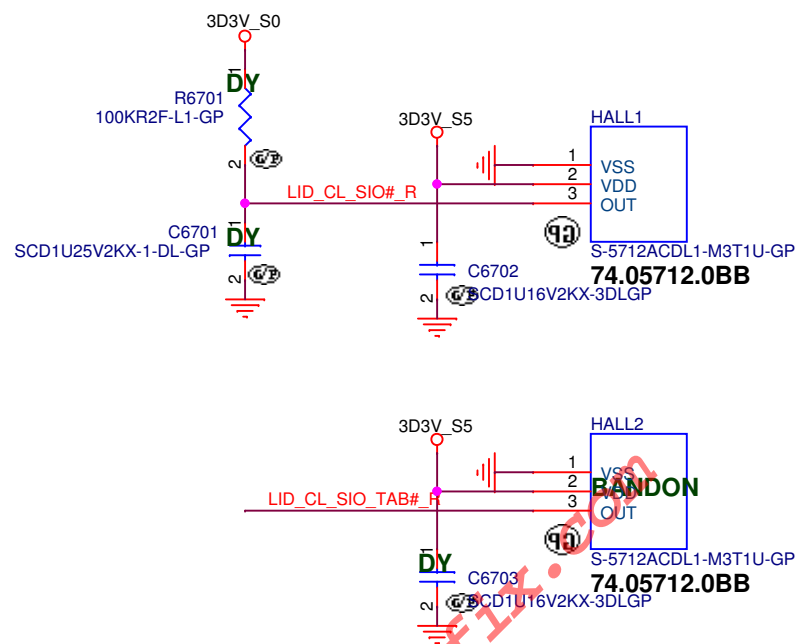
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
------------	---	-------------------

Date: Friday, February 15, 2019 Sheet 66 of 106


Main Func = Sensor (Hall-Sensor)

[24,55,64] LID\_CL\_SIO#\_R << >>—  
[24,64] LID\_CL\_SIO\_TAB#\_R << >>—

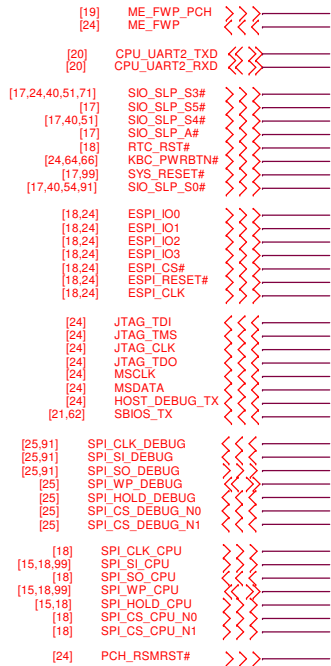
**BANDON**  
**TCS40DLR**  
**[074.TCS40.M001]**  
  
**NORTHBAY**  
**APX8131A**  
**[074.08131.007B]**



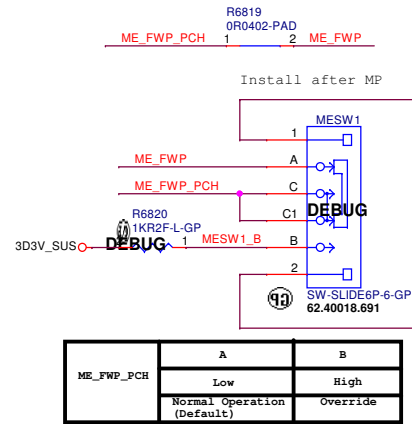
<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Sensor (Hall-Sensor)</b>					
Size A4	Document Number <b>Bandon / NorthBay 13"</b>				Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 67		of 106	

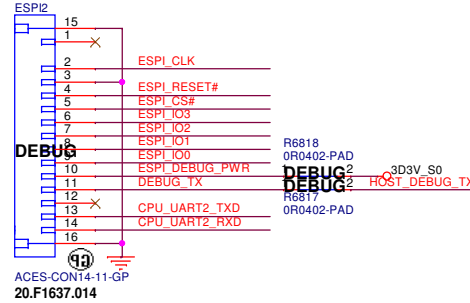
# Main Func = Debug



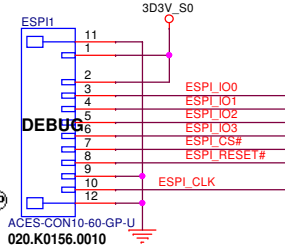
## Firmware SW



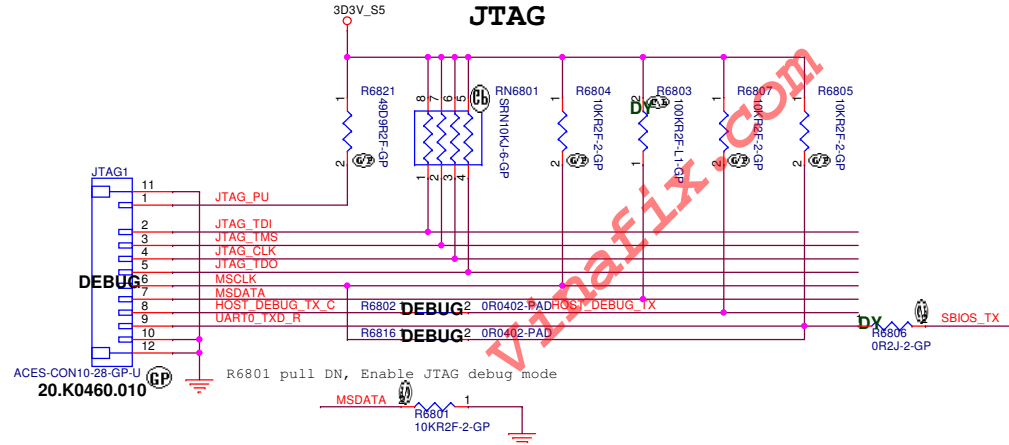
## ESPI DEBUG (Wistron)



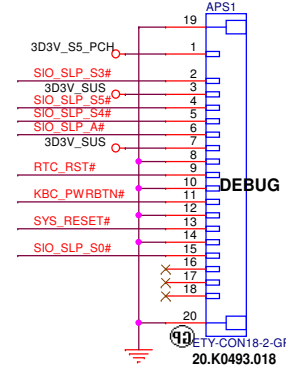
## ESPI DEBUG (DELL)



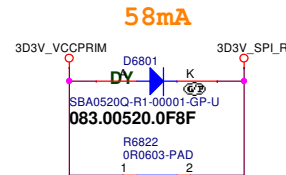
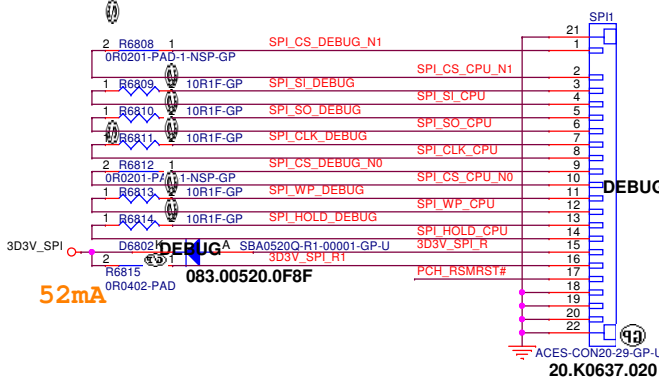
## JTAG



## APS DEBUG



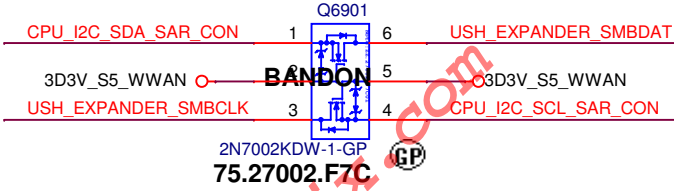
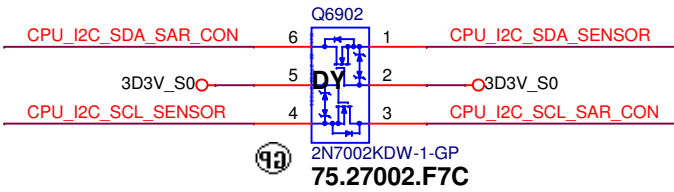
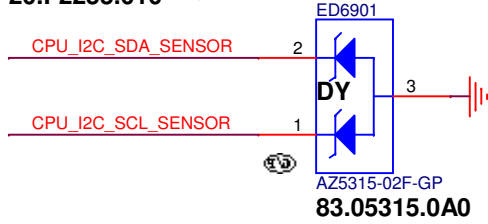
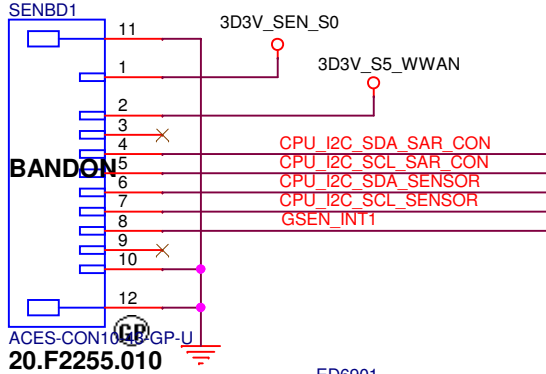
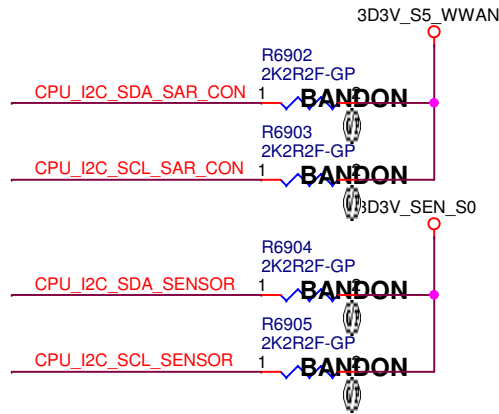
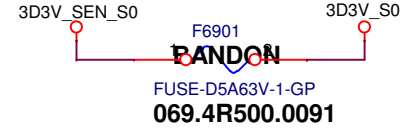
## SPI DEBUG




<Core Design>

Main Func = Sensor (E-compass/A+Gyro/SAR)

[20] GSEN\_INT1 <<< \_\_\_\_\_  
[20,70] CPU\_I2C\_SDA\_SENSOR <<< \_\_\_\_\_  
[20,70] CPU\_I2C\_SCL\_SENSOR <<< \_\_\_\_\_  
[24,66] USH\_EXPANDER\_SMBDAT <<< \_\_\_\_\_  
[24,66] USH\_EXPANDER\_SMBCLK <<< \_\_\_\_\_



<Core Design>



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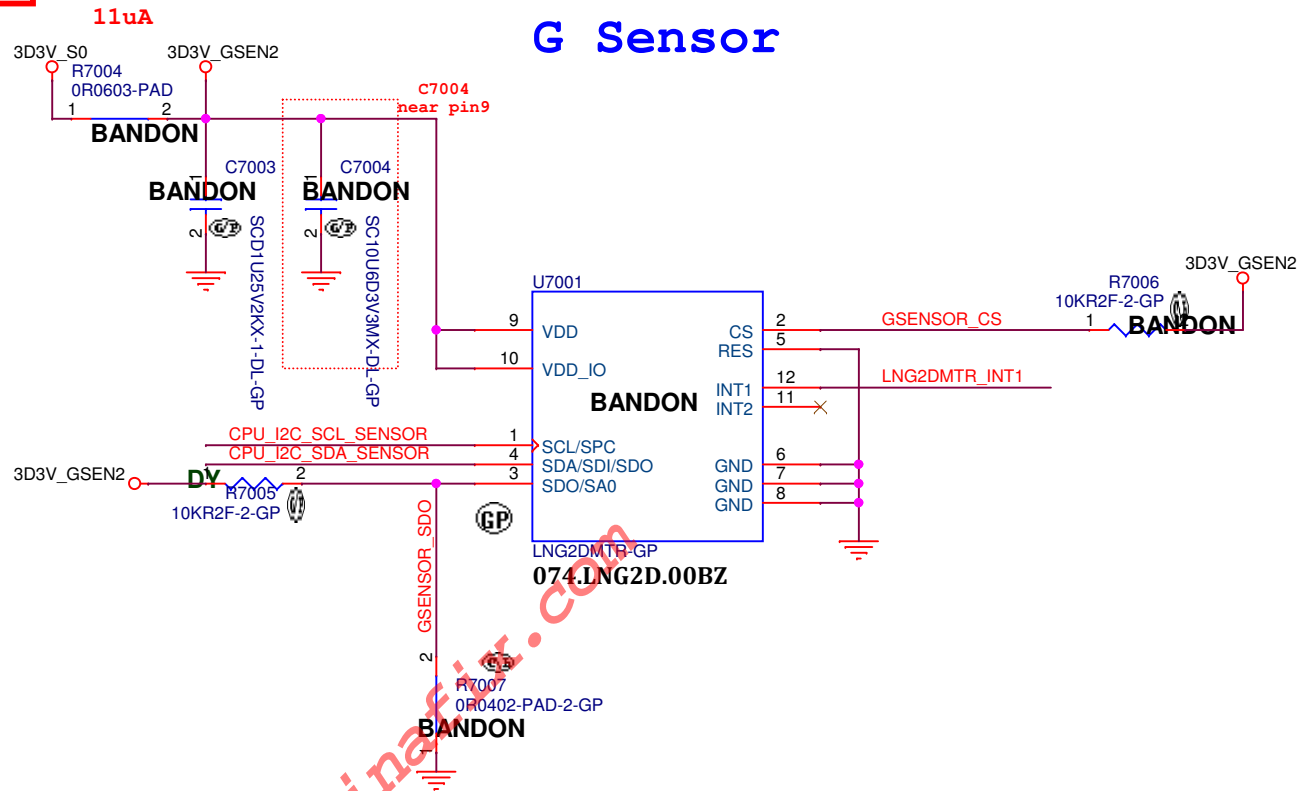
Title  
**Sensor (GYROSCOPE/PRESSUE/ALS)**

Size A4 | Document Number  
**Bandon / NorthBay 13"** | Rev  
**X00**

Date: Friday, February 15, 2019 | Sheet 69 of 106

Main Func = G-sensor

[20,69] CPU\_I2C\_SDA\_SENSOR  
[20,69] CPU\_I2C\_SCL\_SENSOR  
[20] LNG2DMTR\_INT1



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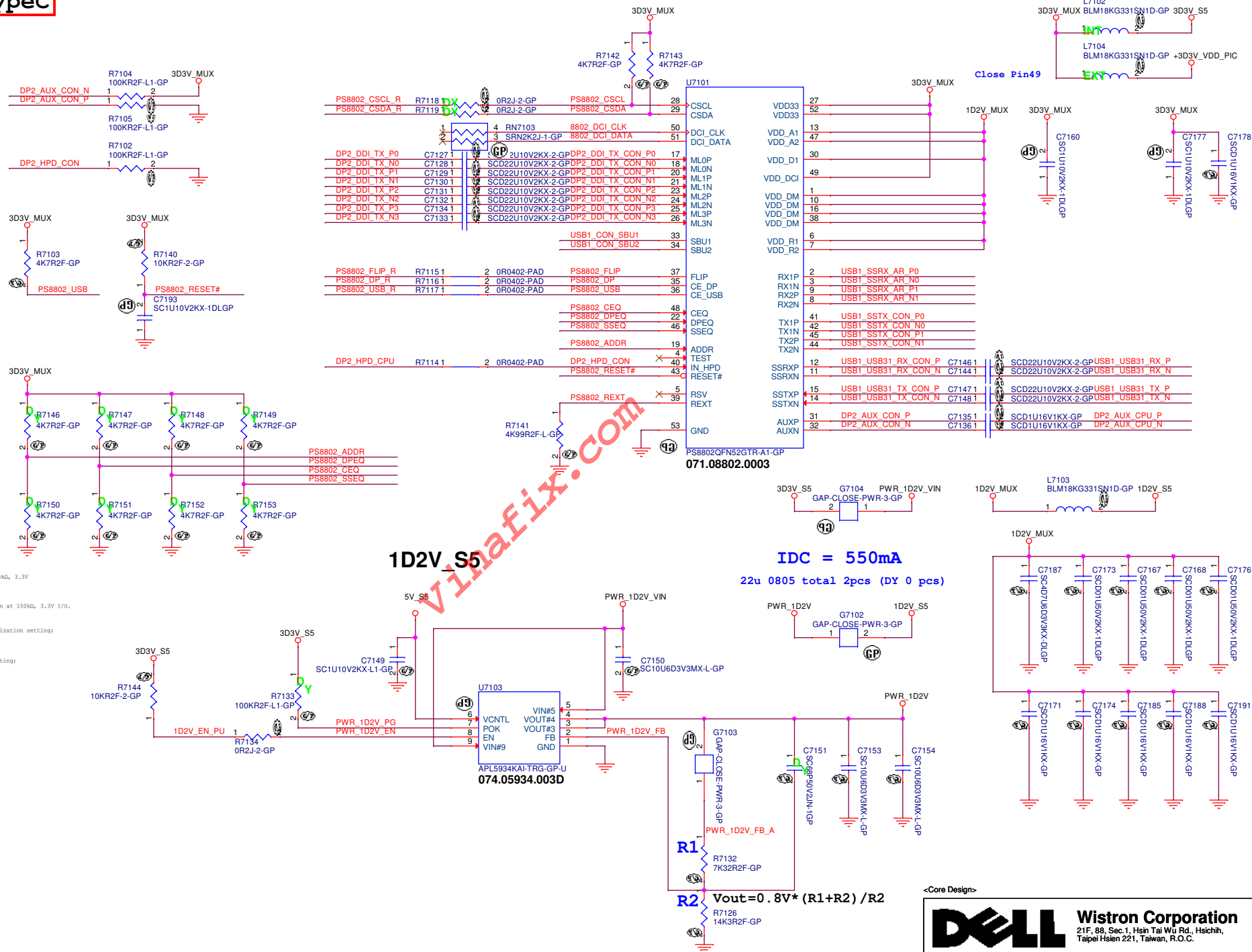
Title			<b>Sensor (G-sensor)</b>	
Size	Document Number	Rev		
A4		<b>Bandon / NorthBay 13"</b>		<b>X00</b>
Date: Friday, February 15, 2019		Sheet	70	of 106

# Main Func = TypeC

## USB1

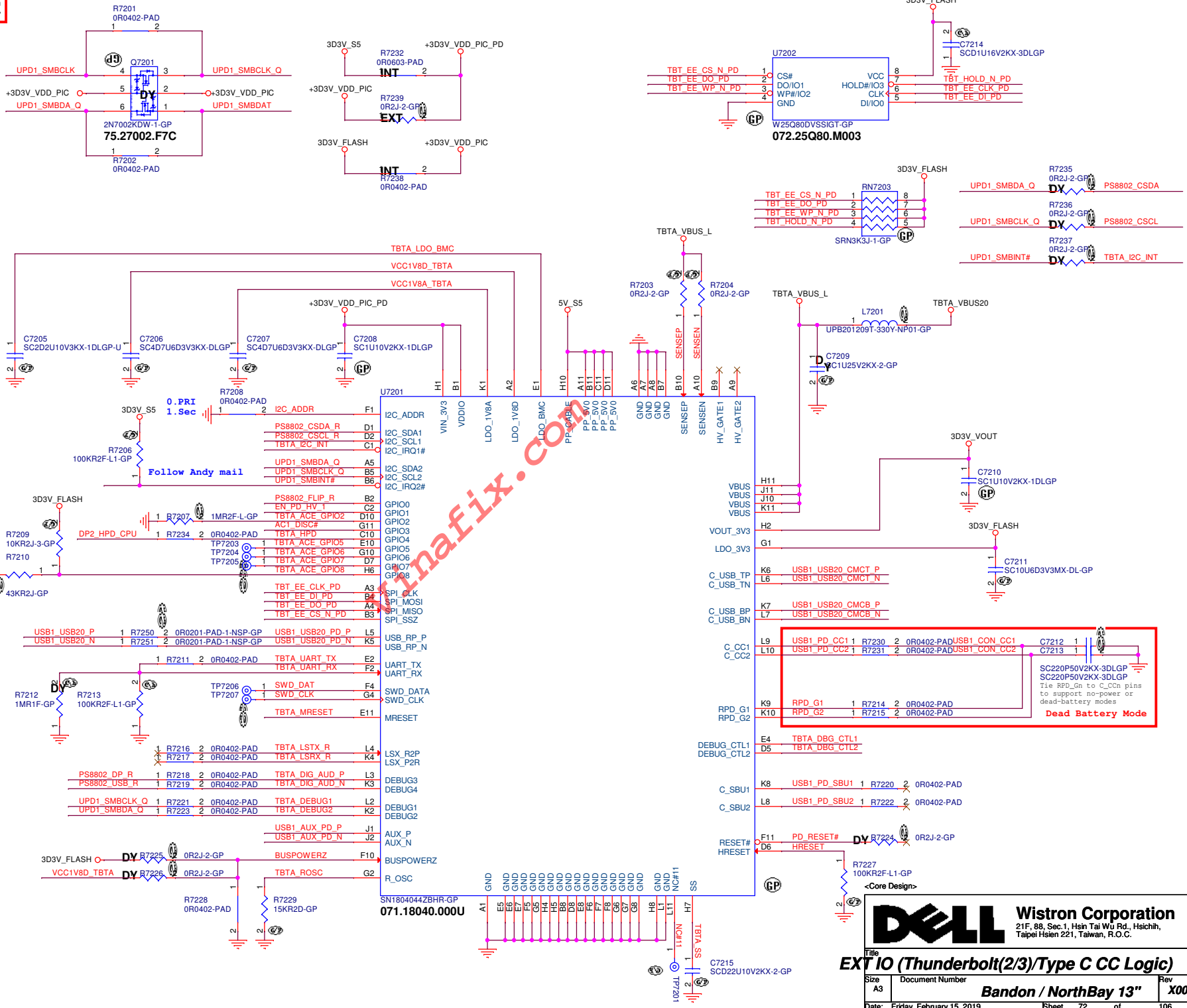
[16]	USB1_USB31_RX_N	>>>
[16]	USB1_USB31_RX_P	>>>
[16]	USB1_USB31_TX_N	>>>
[16]	USB1_USB31_TX_P	>>>
[72]	PS8802_CSDA_R	>>>
[72]	PS8802_C_SCL_R	>>>
[73]	USB1_CON_SBU1	>>>
[73]	USB1_CON_SBU2	>>>
[4]	DP2_DDI_TX_P0	>>>
[4]	DP2_DDI_TX_N0	>>>
[4]	DP2_DDI_TX_P1	>>>
[4]	DP2_DDI_TX_N1	>>>
[4]	DP2_DDI_TX_P2	>>>
[4]	DP2_DDI_TX_N2	>>>
[4]	DP2_DDI_TX_P3	>>>
[4]	DP2_DDI_TX_N3	>>>
[4]	DP2_AUX_CPU_P	>>>
[4]	DP2_AUX_CPU_N	>>>
[4,72]	DP2_HPDC_CPU	<<<
[73]	USB1_SSTX_CON_P0	>>>
[73]	USB1_SSTX_CON_N0	>>>
[73]	USB1_SSTX_CON_P1	>>>
[73]	USB1_SSTX_CON_N1	>>>
[73]	USB1_SSRX_AR_P0	>>>
[73]	USB1_SSRX_AR_N0	>>>
[73]	USB1_SSRX_AR_P1	>>>
[73]	USB1_SSRX_AR_N1	>>>
[72]	PS8802_FLIP_R	>>>
[72]	PS8802_DP_R	>>>
[72]	PS8802_USB_R	>>>
[72]	PS8802_C_SCL	>>>
[72]	PS8802_CSDA	>>>

ADDR: I2C control bus address. Internally pull down at 150kΩ, 3.3V I/O.  
Li: Slave address 0x18-0x1F (default)  
Hi: Slave address 0x20-0x2F (default)  
DP2/DI: DP Receiver equalization settings: Internally pull down at 150kΩ, 3.3V I/O.  
Li: Compensation for channel loss up to 12dB (Default)  
Hi: Compensation for channel loss up to 18dB  
CS2: USB Type-C connector facing Rx channel receiver equalization settings: Internally pull down at 150kΩ, 3.3V I/O.  
Li: Compensation for channel loss up to 16dB (Default)  
Hi: Compensation for channel loss up to 18dB  
SS2: USB Host facing Rx channel receiver equalization settings: Internally pull down at 150kΩ, 3.3V I/O.  
Li: Compensation for channel loss up to 12dB (Default)  
Hi: Compensation for channel loss up to 18dB



# Main Func = TypeC

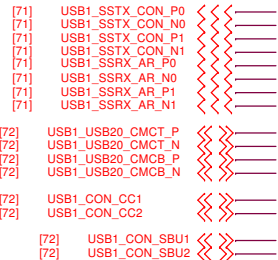
[24]	UPD1_SMBCLK	>>>
[24]	UPD1_SMBDAT	>>>
[24]	UPD1_SMBINT#	>>>
[73]	USB1_CON_CC1	>>>
[73]	USB1_CON_CC2	>>>
[16,72]	USB1_USB20_N	>>>
[16,72]	USB1_USB20_P	>>>
[74]	AC1_DISC#	<<<
[74]	EN_PD_HV_1	<<<
[71]	PS8802_CSDA_R	>>>
[71]	PS8802_C_SCL_R	>>>
[16,72]	USB1_USB20_P	>>>
[16,72]	USB1_USB20_N	>>>
[73]	USB1_USB20_CMCT_P	>>>
[73]	USB1_USB20_CMCT_N	>>>
[73]	USB1_USB20_CMCB_P	>>>
[73]	USB1_USB20_CMCB_N	>>>
[71]	PS8802_C_SCL	>>>
[71]	PS8802_CSDA	>>>
[71,73]	USB1_CON_SBU1	>>>
[71,73]	USB1_CON_SBU2	>>>
[71]	PS8802_FLIP_R	>>>
[71]	PS8802_DP_R	>>>
[71]	PS8802_USB_R	>>>
[4,71]	DP2_HPD_CPU	<<<



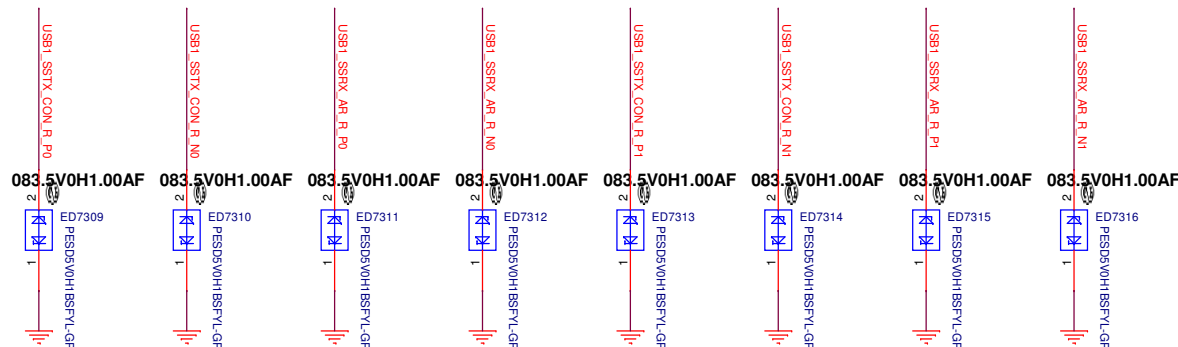
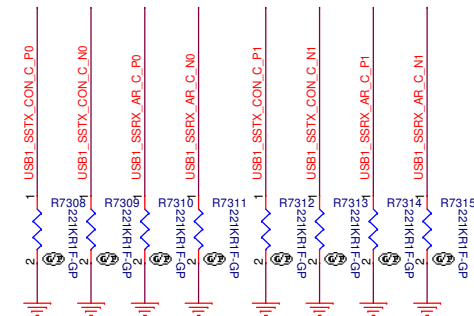
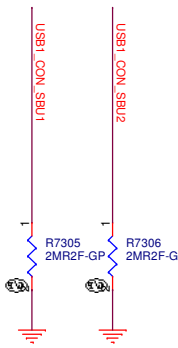
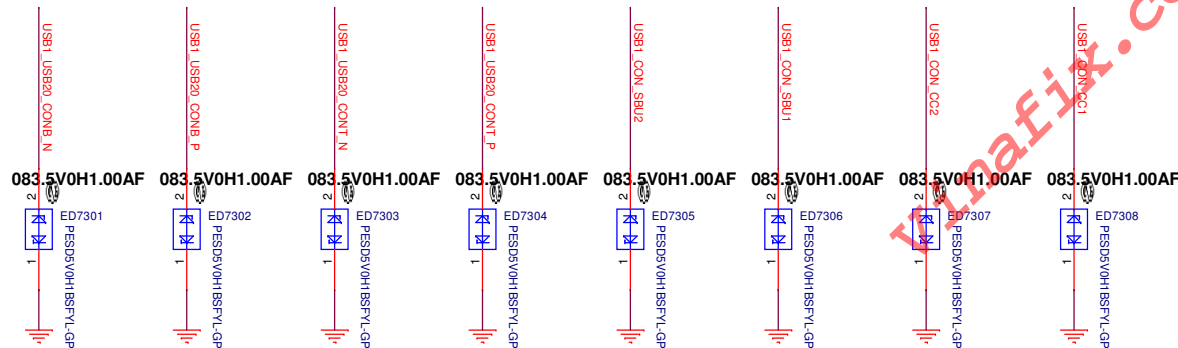
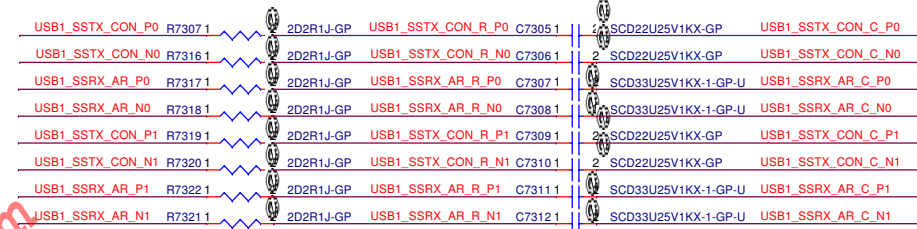
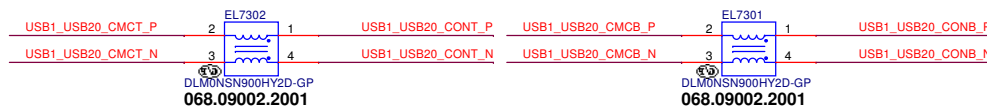
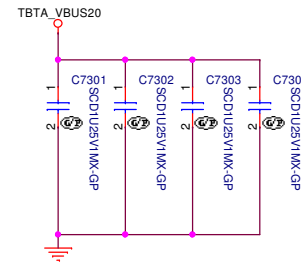
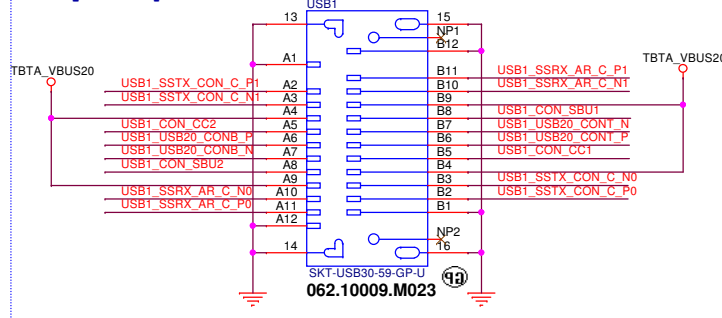


# Main Func = TypeC

## USB1



## For Layout Swap A&B Connection



<Core Design>

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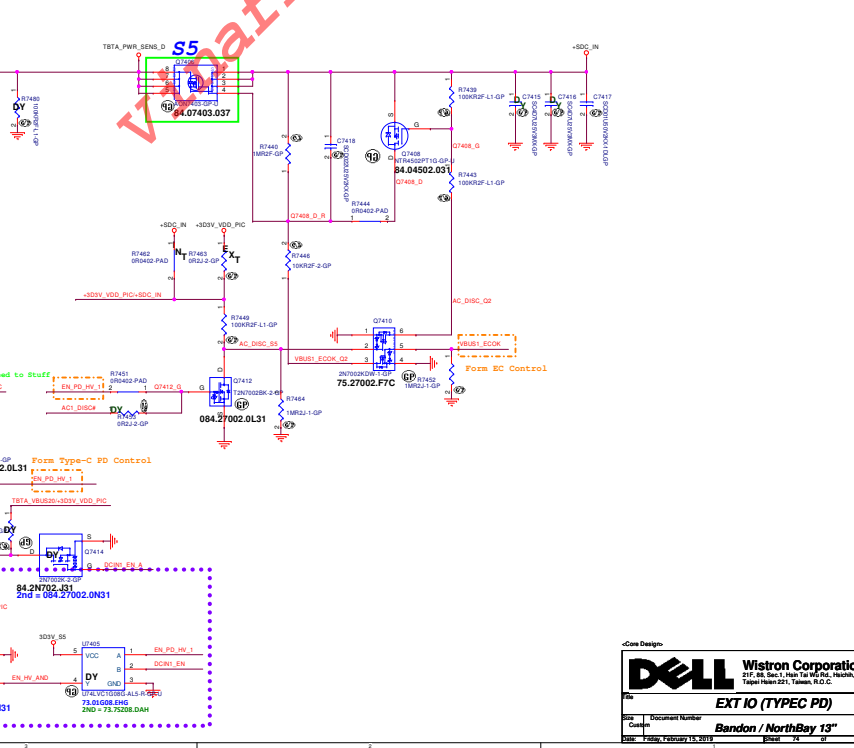
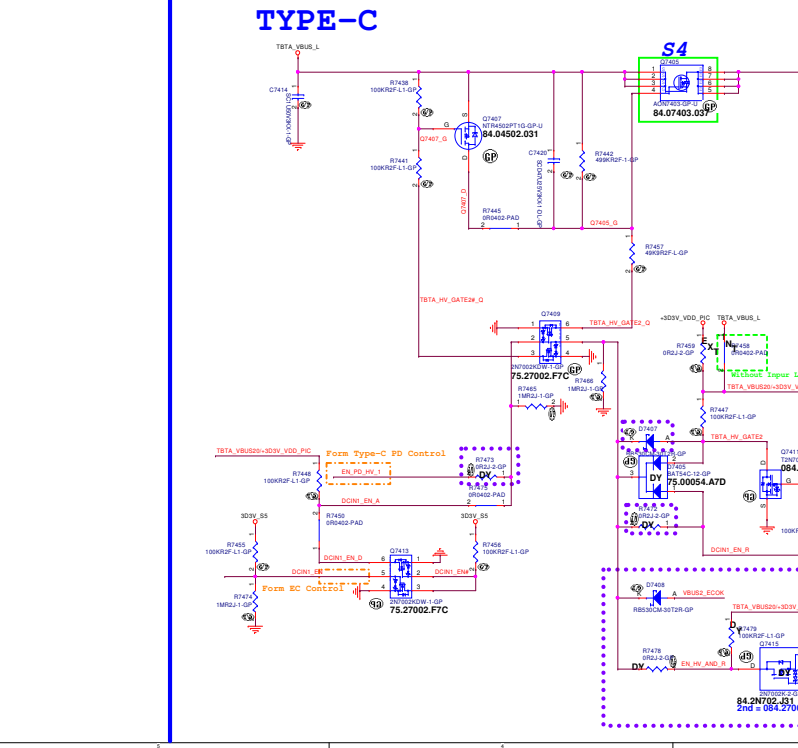
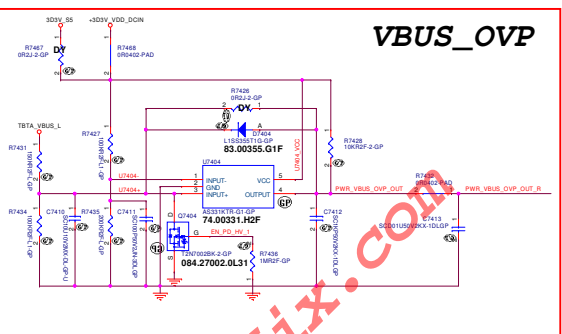
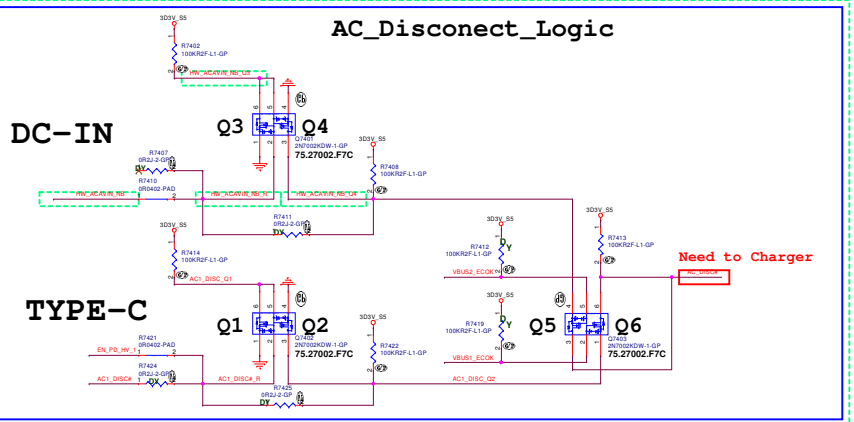
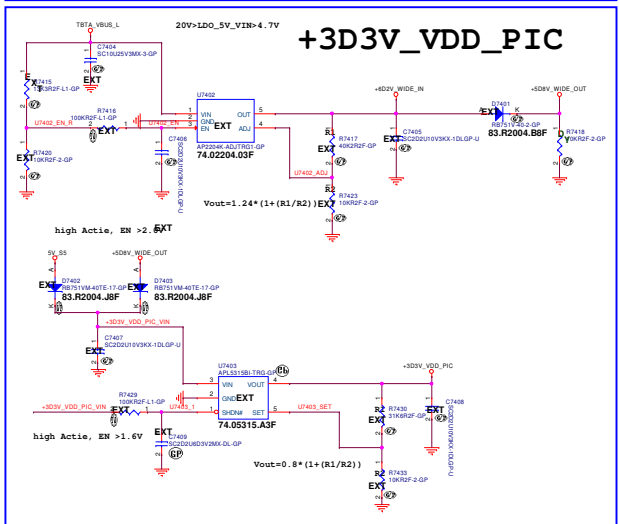
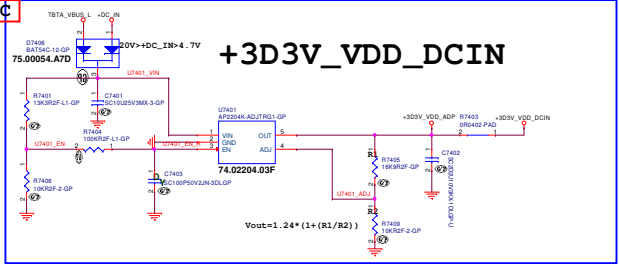
Title  
**EXT IO (Thunderbolt(3/3)/Type C Conn)**

Size A3 Document Number **Bandon / NorthBay 13"** Rev **X00**

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Main Func = TypeC

- [P4444] HW\_ACAPN\_00 >>>
- [75] AC1\_DISC >>>
- [P443] VBUS1\_ECON >>>
- [79] EN\_PD\_HV\_1 >>>
- [P443] AC\_DISC >>>
- [P4] DCIN\_EN >>>
- [H3] PWR\_VBUS\_OVP\_OUT\_R <<<
- [P444] VBUS2\_ECON <<<




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Title <b>EXT IO (RSVD)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 75 of	106


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<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>GPU (RSVD) (PEG 1/5)</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 76		of 106	


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Title <b>GPU (RSVD) (DIGITAL 2/5)</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 77		of 106	


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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>GPU (RSVD) (VRAM 3/5)</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 78 of 106


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Title <b>GPU (RSVD) (GPIO 4/5)</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 79 of 106

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Title <b>GPU (RSVD) (PWR/GND 5/5)</b>					
Size A4	Document Number <b>Bandon / NorthBay 13"</b>				Rev <b>X00</b>
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			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>GPU (RSVD) (VRAM1,2 1/4)</b>					
Size A4	Document Number <b>Bandon / NorthBay 13"</b>				Rev <b>X00</b>
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			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>GPU (RSVD) (VRAM3,4 2/4)</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
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<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>GPU (RSVD) (VRAM5,6 3/4)</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
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			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>GPU (RSVD) (VRAM7,8 4/4)</b>					
Size A4	Document Number <b>Bandon / NorthBay 13"</b>				Rev <b>X00</b>
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<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>GPU (RSVD) (VGA_CORE)</b>					
Size A4	Document Number <b>Bandon / NorthBay 13"</b>				Rev <b>X00</b>
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>GPU (RSVD) (Sequence)</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
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<Core Design>

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Title <b>GPU (RSVD)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
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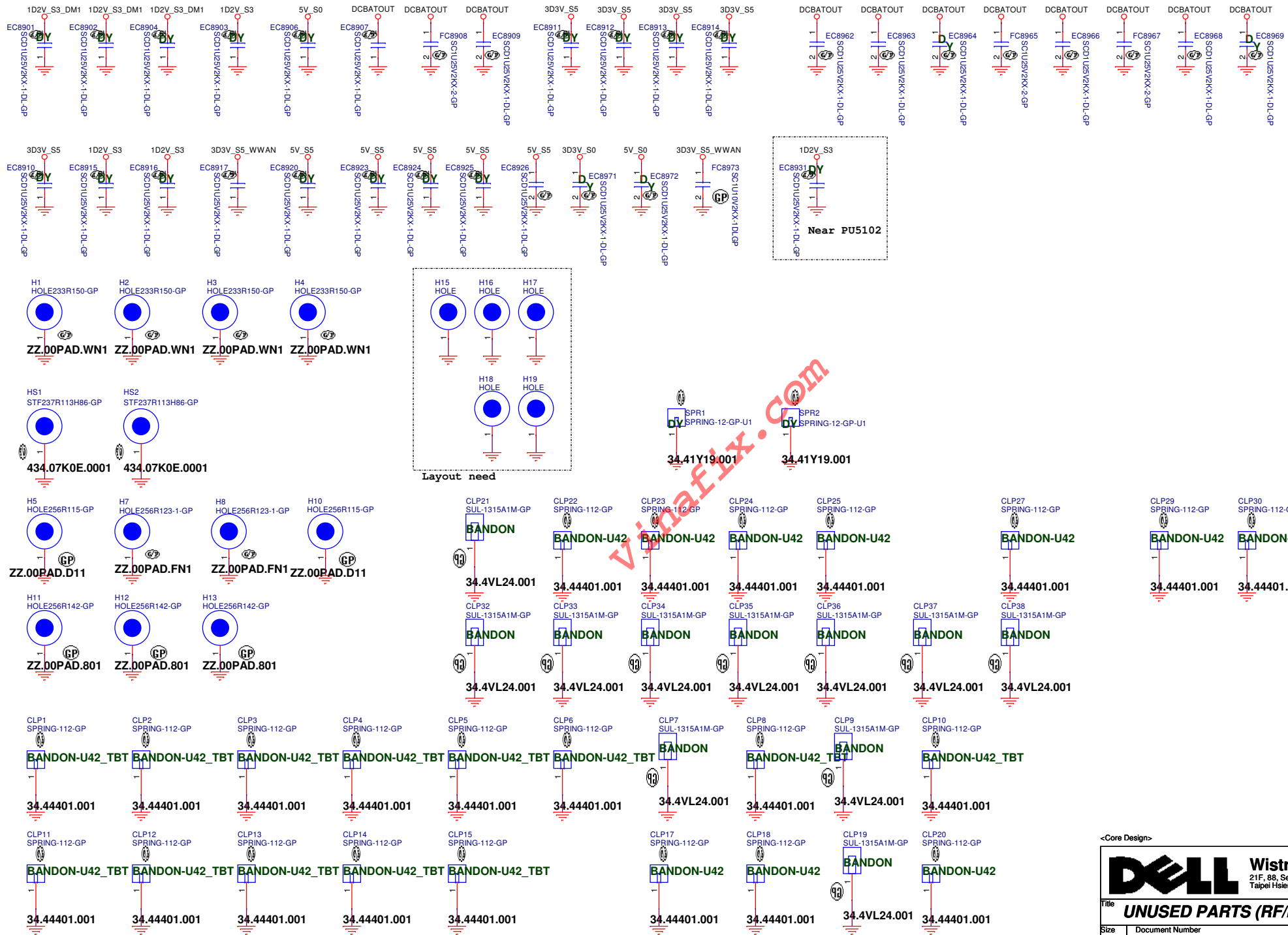
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>UNUSED PARTS (RSVD)</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
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**Main Func = EMC/ RF**



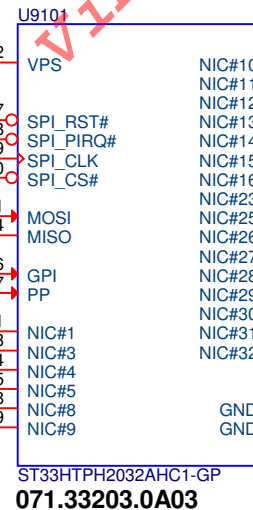
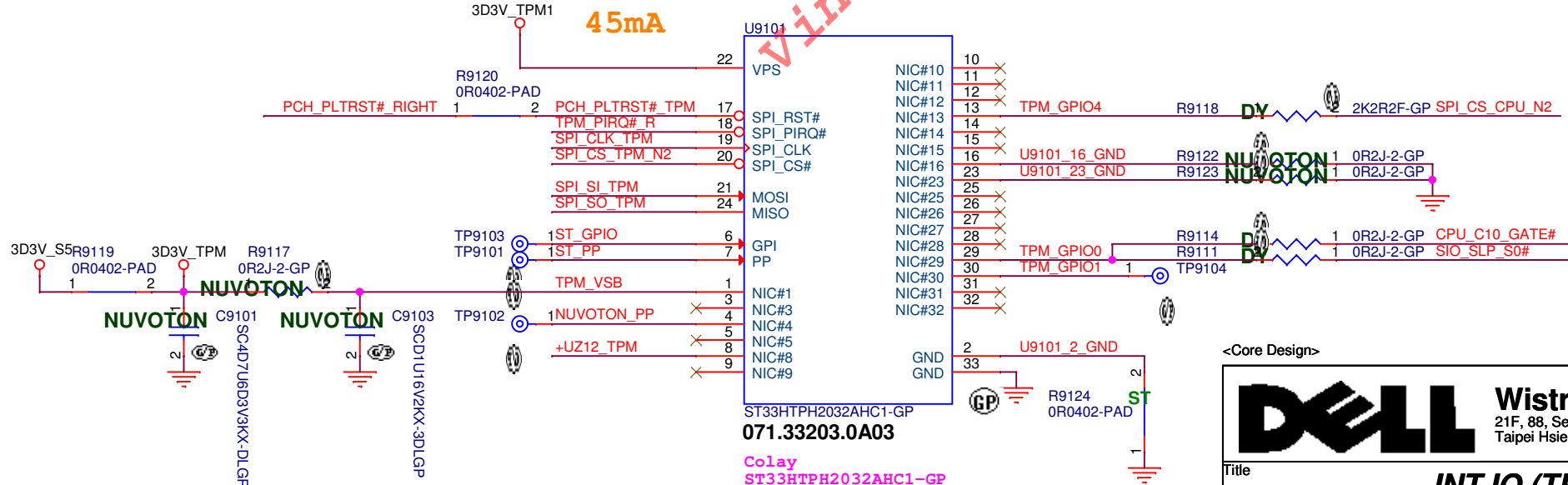
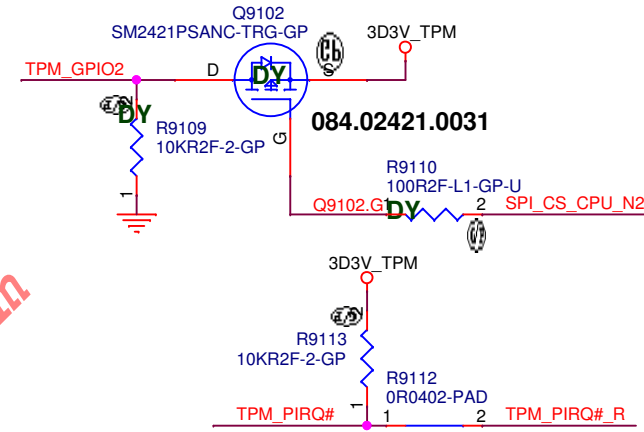
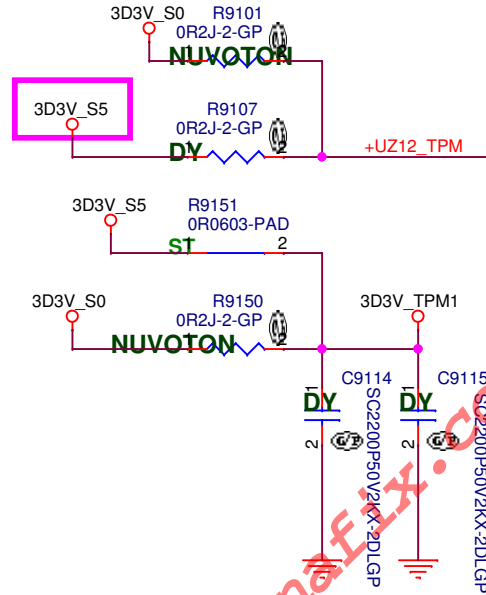
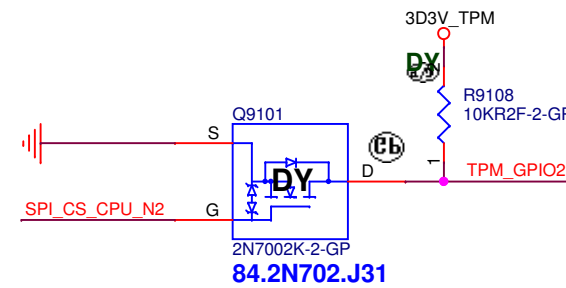
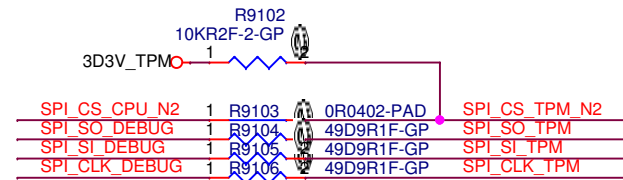
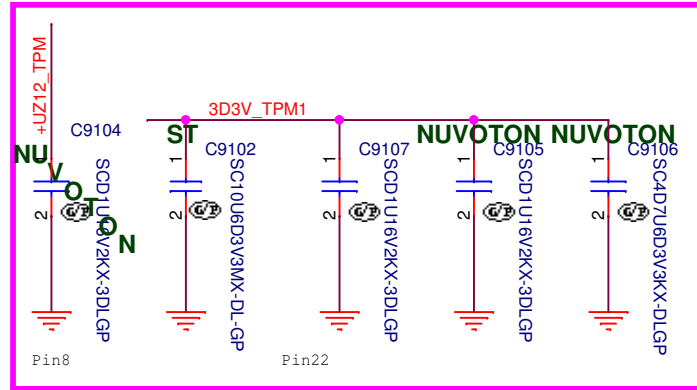
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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>INT IO (RSVD) (NFC)</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
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# Main Func = TPM

[20]	TPM_PIRQ#	
[17,40,54,68]	SIO_SLP_S0#	
[17,33,61,62,97]	PCH_PLTRST#_RIGHT	
[25,68]	SPI_CLK_DEBUG	
[25,68]	SPI_SI_DEBUG	
[25,68]	SPI_SO_DEBUG	
[18]	SPI_CS_CPU_N2	
[21,24,40,54]	CPU_C10_GATE#	



Colay  
ST33HTPH2032AHC1-GP  
071.33203.0A03  
NPCT750JAAYX-1-GP  
071.00750.M001

<Core Design>

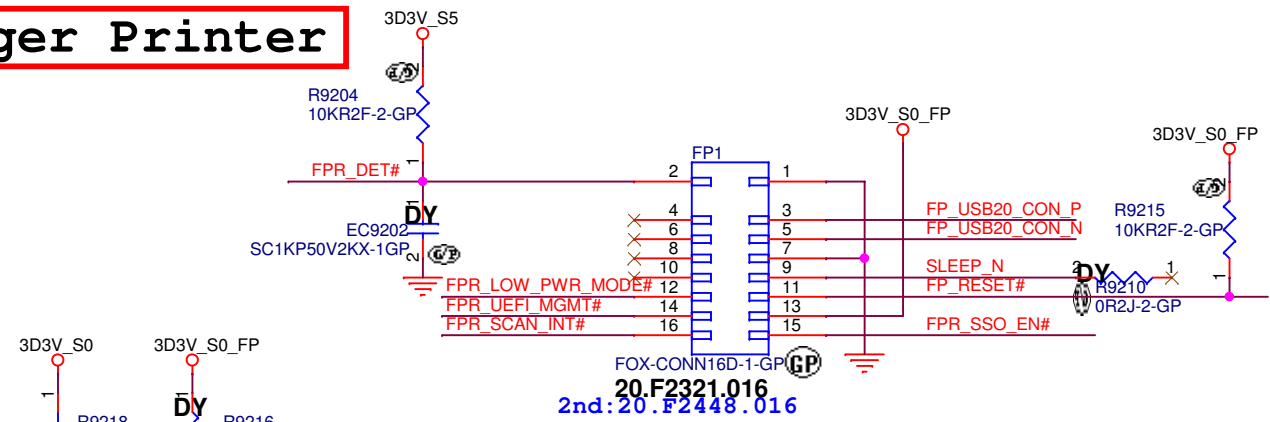


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Taipei Hsien 221, Taiwan, R.O.C.

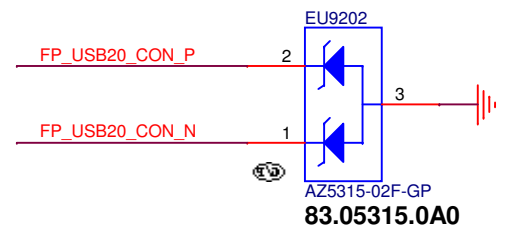
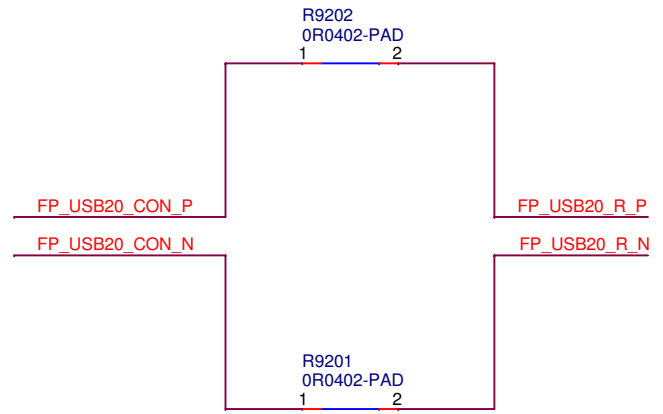
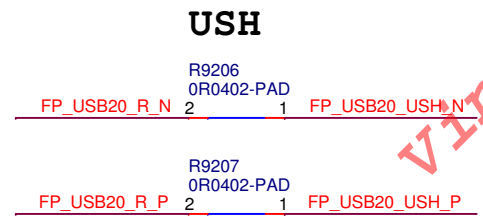
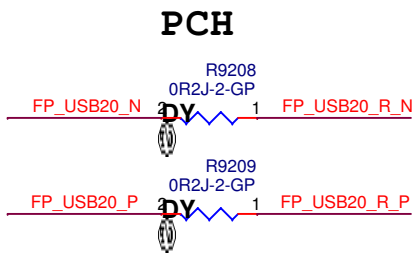
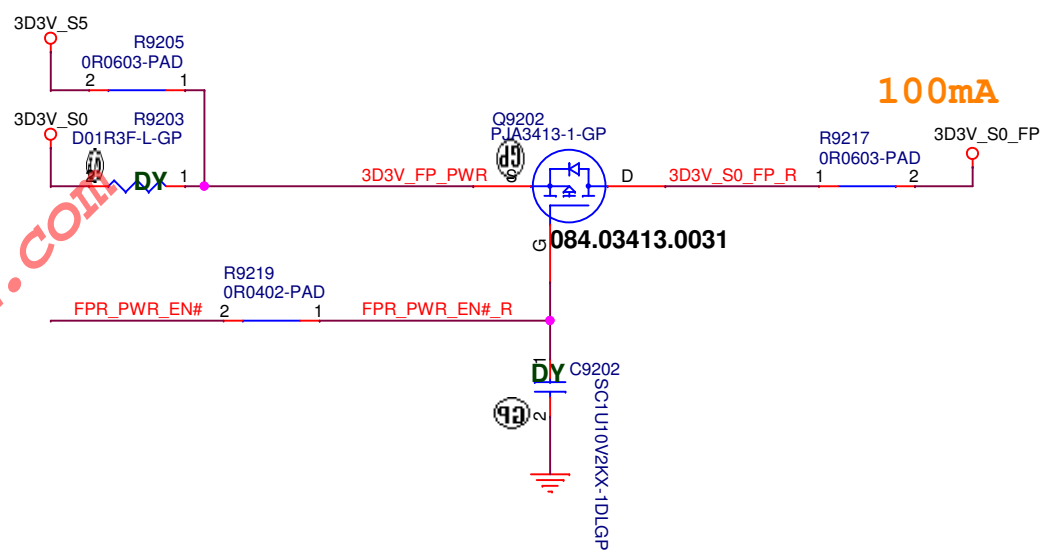
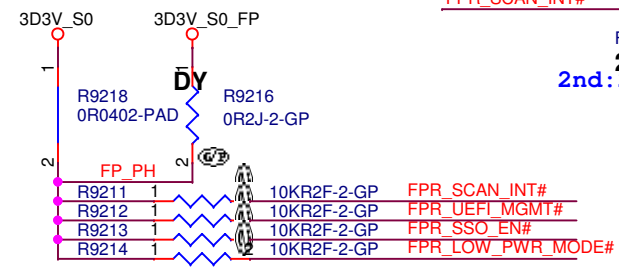
Title			INT IO (TPM)	
Size	Document Number	Bandon / NorthBay 13"		Rev
A4				X00
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Main Func = Finger Printer

- [16] FP\_USB20\_N
- [16] FP\_USB20\_P
- [24,64] FPR\_DET#
- [66] FP\_USB20\_USH\_N
- [66] FP\_USB20\_USH\_P
- [24] FPR\_PWR\_EN#
- [24,66] FPR\_SCAN\_INT#
- [24] FPR\_SSO\_EN#
- [24] FPR\_UEFI\_MGMT#
- [24] FPR\_LOW\_PWR\_MODE#
- [66] FP\_RESET#



Pin 1	GND
Pin 2	FPR_DET(GND)
Pin 3	USB_DP
Pin 4	NA
Pin 5	USB_DM
Pin 6	NA
Pin 7	GND
Pin 8	NA
Pin 9	RESERVED
Pin 10	NA
Pin 11	FP_RESET#
Pin 12	LOW POW MODE#
Pin 13	VDD CHICLET
Pin 14	UEFI_MGMT#
Pin 15	SSO_EN#
Pin 16	FPR_SCAN_INTR#



<Core Design>


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Title: **INT IO (Finger Printer)**

Size: A4	Document Number: <b>Bandon / NorthBay 13"</b>	Rev: <b>X00</b>
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			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>EXT IO (RSVD) (Express Card/PCIE slot)</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
Date: Friday, February 15, 2019			Sheet 93 of 106		


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Title <b>EXT IO (RSVD) (Smart Card/COM/PS2)</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
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Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
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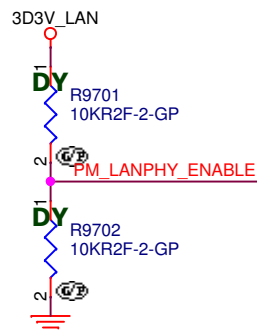
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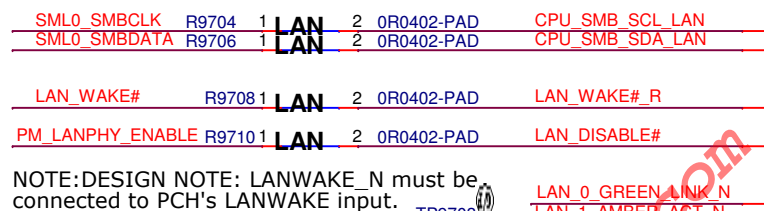
			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Commercial (RSVD) (SW GFX eDP)</b>					
Size A4		Document Number <b>Bandon / NorthBay 13"</b>			Rev <b>X00</b>
Date: Friday, February 15, 2019		Sheet 96		of 106	



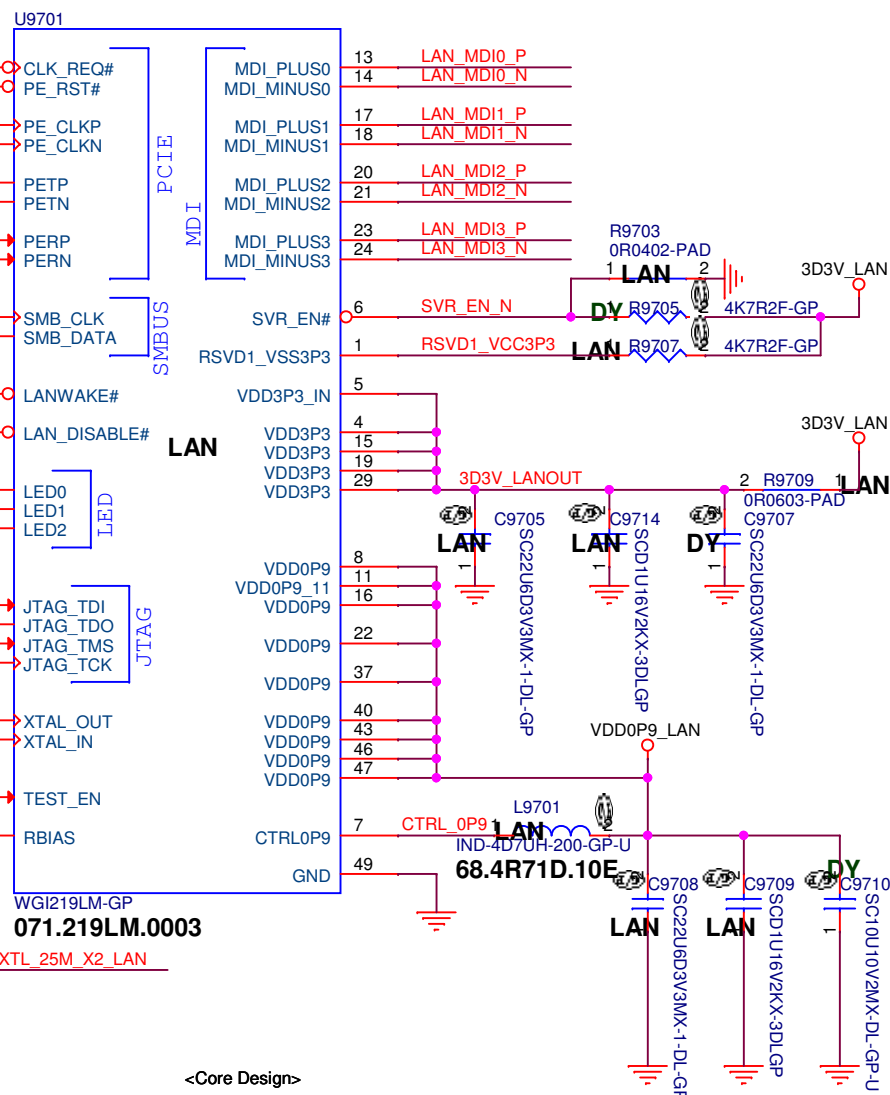
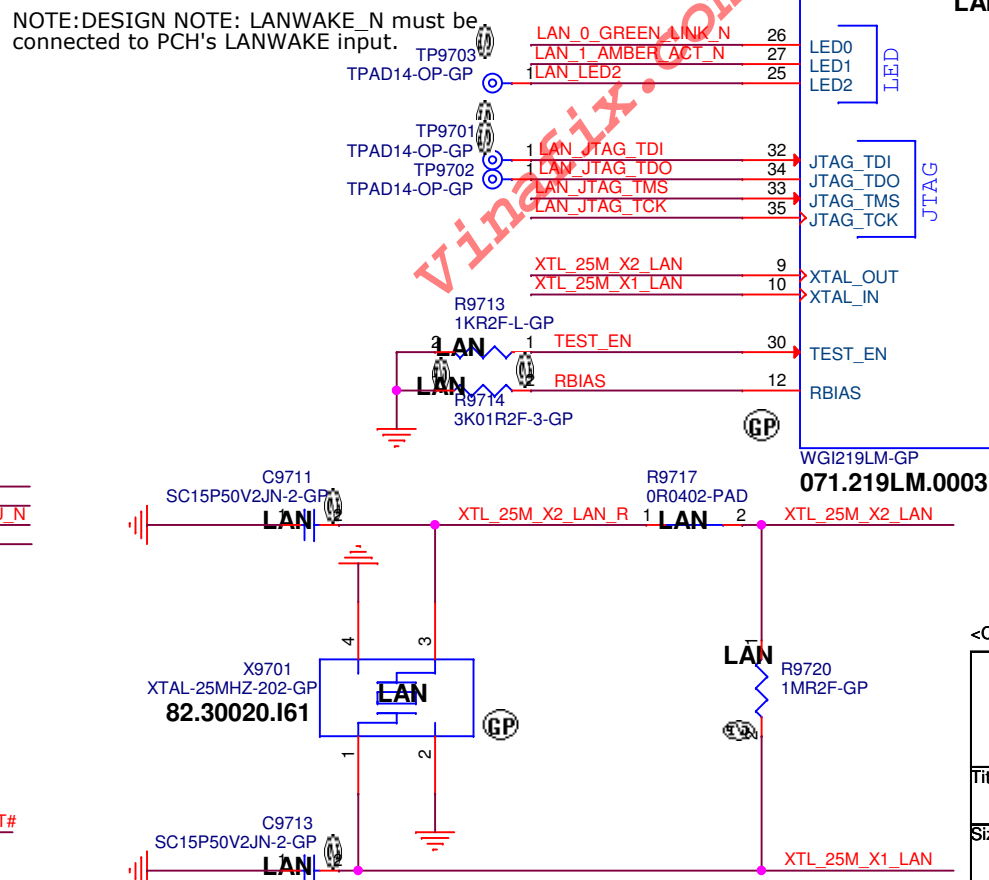
## LAN



LAN_PCIE_RX_P	C9701	LAN	SCD1U16V2KX-3DLGP	LAN_PCIE_RX_C_P
LAN_PCIE_RX_N	C9702	LAN	SCD1U16V2KX-3DLGP	LAN_PCIE_RX_C_N
LAN_PCIE_TX_P	C9703	LAN	SCD1U16V2KX-3DLGP	LAN_PCIE_TX_C_P
LAN_PCIE_TX_N	C9704	LAN	SCD1U16V2KX-3DLGP	LAN_PCIE_TX_C_N



NOTE:DESIGN NOTE: LANWAKE\_N must be connected to PCH's LANWAKE input.



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### **Commercial (Intel LAN)**


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Title <b>Commercial (LAN Switch)</b>			
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# Main Func = Debug (MIPI)

[6] CFG0 >>>-

[6] CFG1 >>>-

[6] CFG2 >>>-

[6] CFG3 >>>-

[6] CFG4 >>>-

[6] CFG5 >>>-

[6] CFG6 >>>-

[6] CFG7 >>>-

[6] CFG8 >>>-

[6] CFG9 >>>-

[6] CFG10 >>>-

[6] CFG11 >>>-

[6] CFG12 >>>-

[6] CFG13 >>>-

[6] CFG14 >>>-

[6] CFG15 >>>-

[6] CFG16 >>>-

[6] CFG17 >>>-

[6] CFG18 >>>-

[6] CFG19 >>>-

[3] BPM\_N0 >>>-

[3] BPM\_N1 >>>-

[6,15] ITP\_PMODE >>>-

[18] XDP\_CLK\_CPU\_N <<<-

[18] XDP\_CLK\_CPU\_P <<<-

[3] PCH\_JTAG\_TCK <<<-

[3] CPU\_JTAG\_PRDY# <<<-

[3] CPU\_JTAG\_PREQ# <<<-

[3] CPU\_JTAG\_TRST# <<<-

[3] CPU\_JTAG\_TCK <<<-

[3] CPU\_JTAG\_TDI <<<-

[3] CPU\_JTAG\_TDO <<<-

[3] CPU\_JTAG\_TMS <<<-

[17,68] SYS\_RESET# >>>-

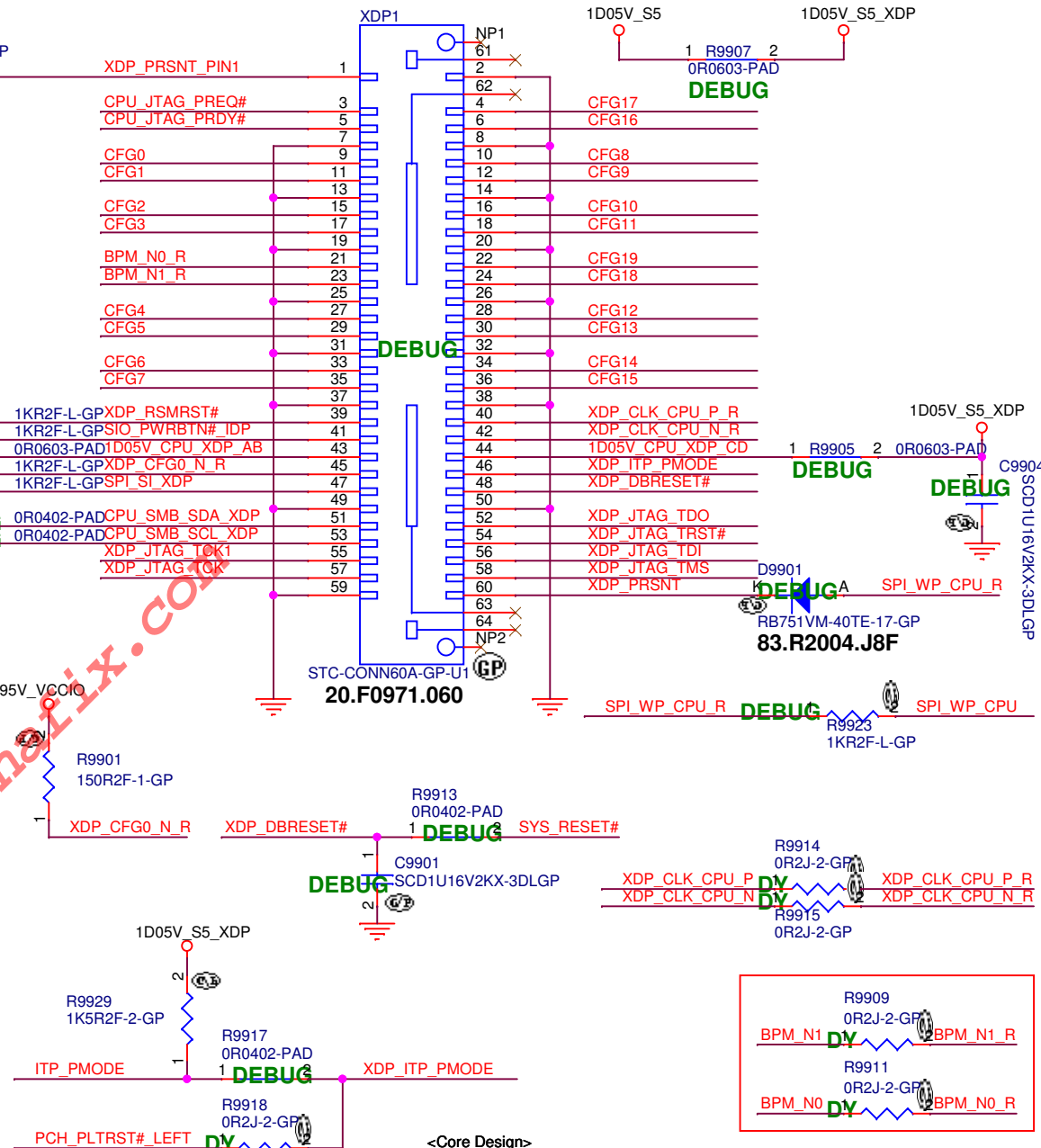
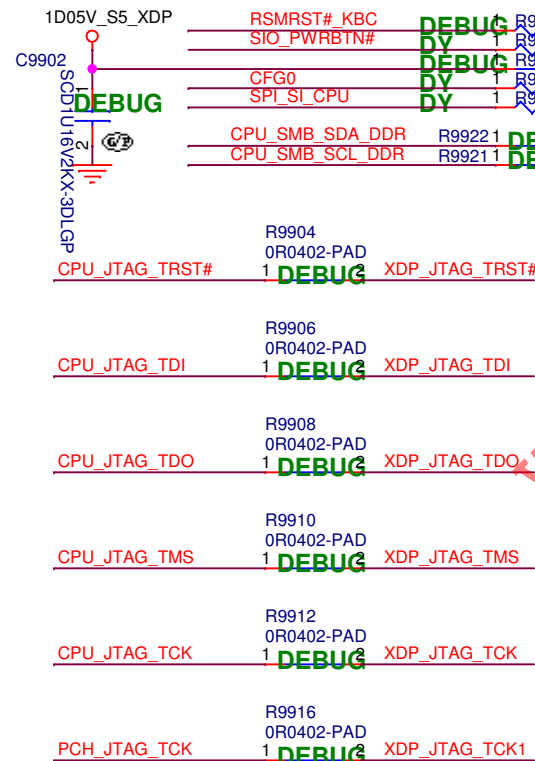
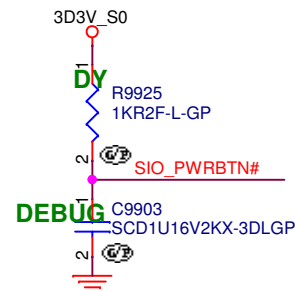
[17,24] SIO\_PWRBTN# >>>-

[12,13,18] CPU\_SMB\_SCL\_DDR <<<-

[12,13,18] CPU\_SMB\_SDA\_DDR <<<-

[17,63,71] PCH\_PLTRST#\_LEFT >>>-

[17,24,64] RSMRST#\_KBC <<<-



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Title				<b>Debug (XDP debug)</b>			
Size		Document Number			Rev		
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# Table of Content

## RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance  
 For the value, it can be read by the number before R. (R means resistor)  
 For the tolerance, it can be read from the last letter.  
 For the rating, we don't show on the symbol name.  
 For the size, R2=>0402, R3=>0603, R5=>0805,....

## CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is  
 Capacitor type + value + rating + size + tolerance + material  
 SCD1U10V2MX-1  
 SC=> SMT Ceramic, TC=> POS cap or SP cap  
 D1U => 0.1uF  
 10V => the voltage rating is 10V  
 2=> 0402, 3=>0603, 5=>0805  
 M=>tolerance M, K, Z  
 X=> X7R/X5R, Y=> Y5V  
 -1 => symbol version, nonsense to EE characteristic

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Title <b>Table of Content</b>		
Size A4	Document Number <b>Bandon / NorthBay 13"</b>	Rev <b>X00</b>
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*Change notes -*

[illegible]

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1	Title

## ***Change History***

Size	A3
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Document Number
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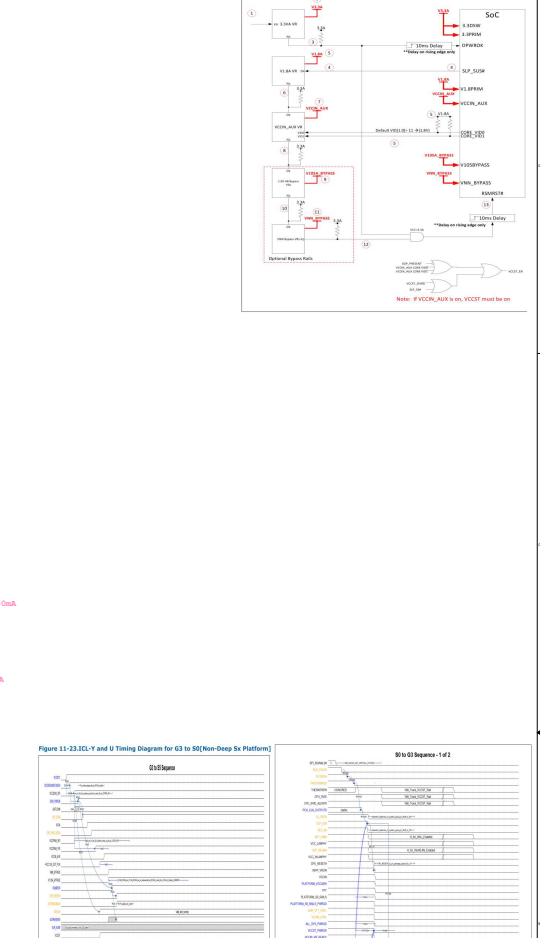
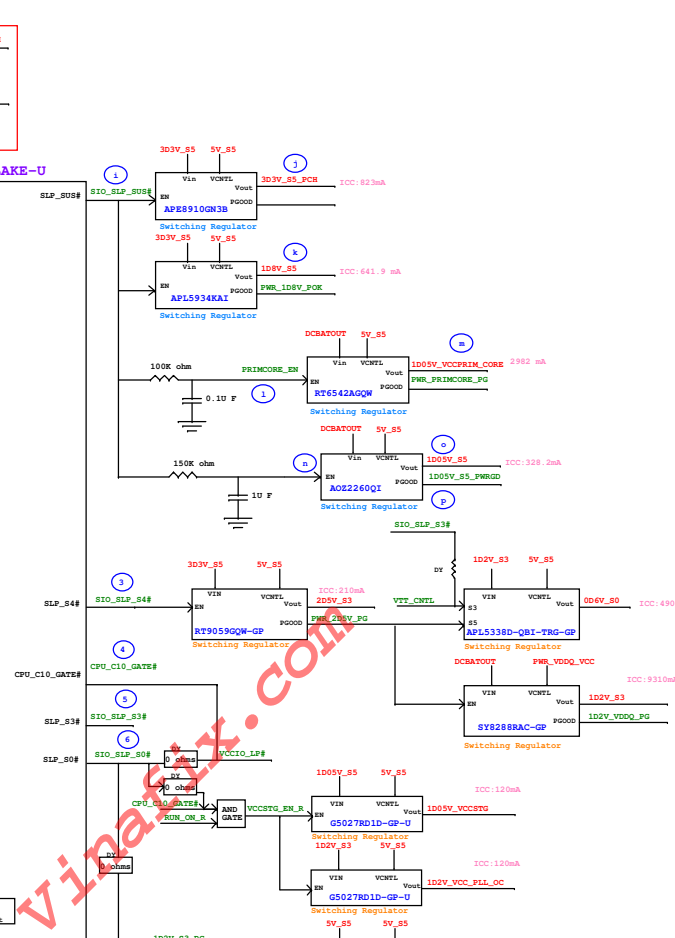
**Bandon / NorthBay 13"**

Rev	X00
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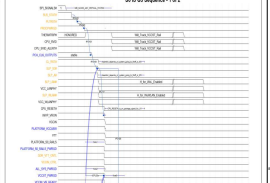
Date: Friday, February 15, 2019

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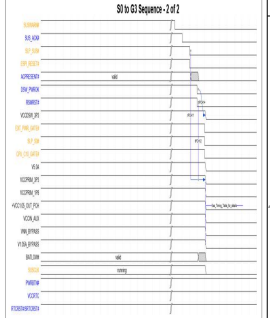
00 to 03 Sequence - 1 of 3



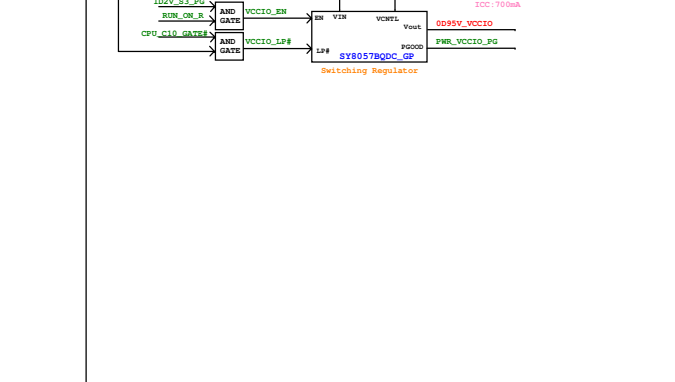
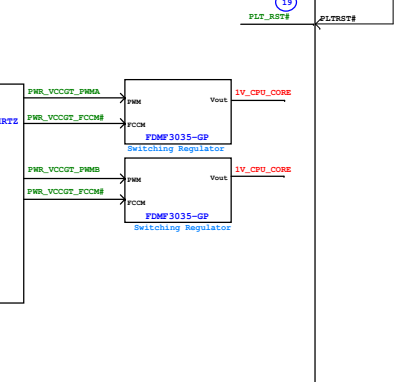
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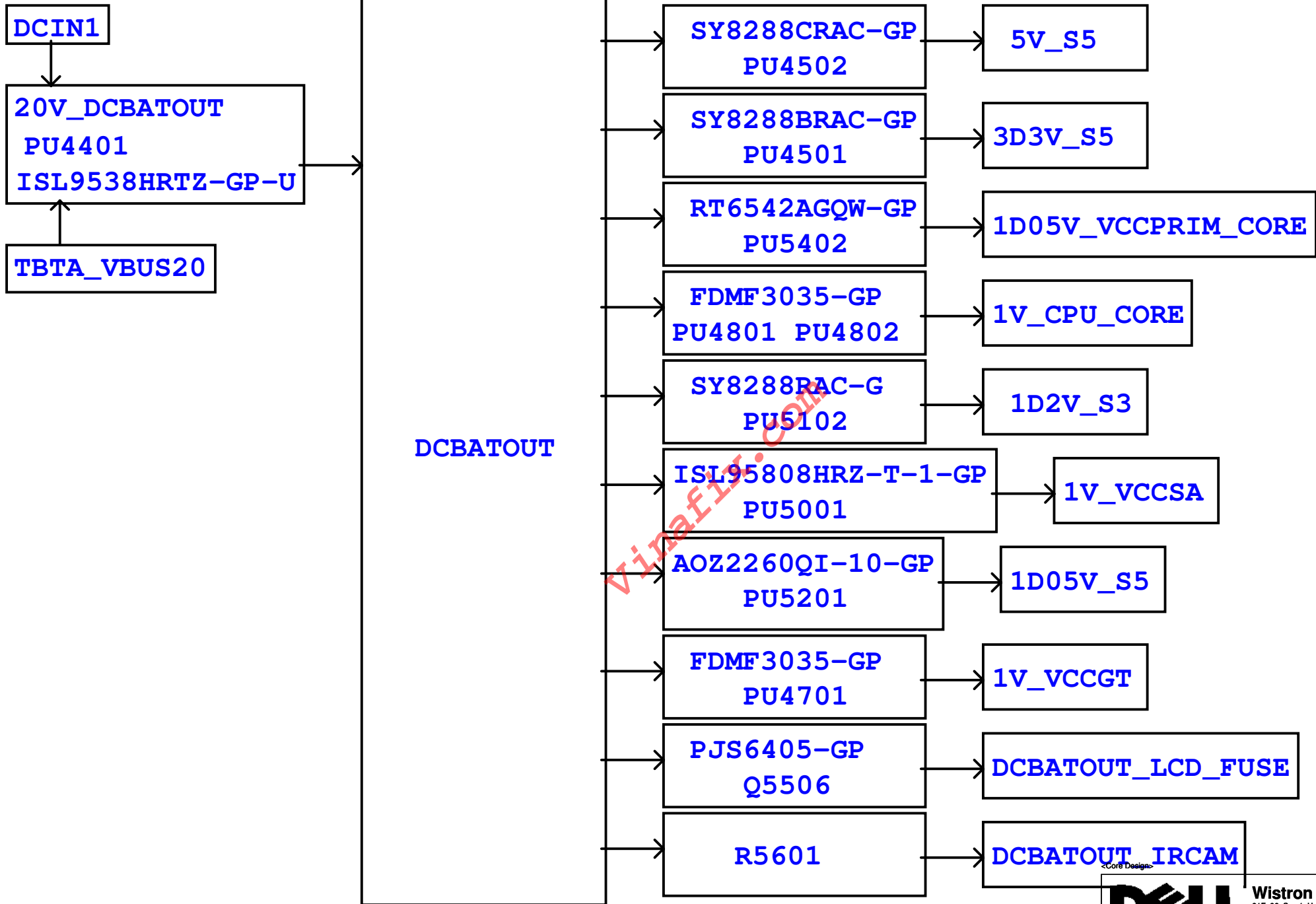
- These are all the processor and SoC core calls. Includes the calls like 3.3.4.5-c platform calls, etc.
- This represents the unused Power Good signal, including the platform calls mentioned in Note (1).
- Signal may change before or after `SWR_364_365_367_368_369_370_371_372_373_374_375_376_377_378_379_380_381_382_383_384_385_386_387_388_389_390_391_392_393_394_395_396_397_398_399_400_401_402_403_404_405_406_407_408_409_410_411_412_413_414_415_416_417_418_419_420_421_422_423_424_425_426_427_428_429_430_431_432_433_434_435_436_437_438_439_440_441_442_443_444_445_446_447_448_449_450_451_452_453_454_455_456_457_458_459_460_461_462_463_464_465_466_467_468_469_470_471_472_473_474_475_476_477_478_479_480_481_482_483_484_485_486_487_488_489_490_491_492_493_494_495_496_497_498_499_500_501_502_503_504_505_506_507_508_509_510_511_512_513_514_515_516_517_518_519_520_521_522_523_524_525_526_527_528_529_530_531_532_533_534_535_536_537_538_539_540_541_542_543_544_545_546_547_548_549_550_551_552_553_554_555_556_557_558_559_560_561_562_563_564_565_566_567_568_569_570_571_572_573_574_575_576_577_578_579_580_581_582_583_584_585_586_587_588_589_590_591_592_593_594_595_596_597_598_599_600_601_602_603_604_605_606_607_608_609_610_611_612_613_614_615_616_617_618_619_620_621_622_623_624_625_626_627_628_629_630_631_632_633_634_635_636_637_638_639_640_641_642_643_644_645_646_647_648_649_650_651_652_653_654_655_656_657_658_659_660_661_662_663_664_665_666_667_668_669_670_671_672_673_674_675_676_677_678_679_680_681_682_683_684_685_686_687_688_689_690_691_692_693_694_695_696_697_698_699_700_701_702_703_704_705_706_707_708_709_710_711_712_713_714_715_716_717_718_719_720_721_722_723_724_725_726_727_728_729_730_731_732_733_734_735_736_737_738_739_740_741_742_743_744_745_746_747_748_749_750_751_752_753_754_755_756_757_758_759_760_761_762_763_764_765_766_767_768_769_770_771_772_773_774_775_776_777_778_779_780_781_782_783_784_785_786_787_788_789_790_791_792_793_794_795_796_797_798_799_800_801_802_803_804_805_806_807_808_809_810_811_812_813_814_815_816_817_818_819_820_821_822_823_824_825_826_827_828_829_830_831_832_833_834_835_836_837_838_839_840_841_842_843_844_845_846_847_848_849_850_851_852_853_854_855_856_857_858_859_860_861_862_863_864_865_866_867_868_869_870_871_872_873_874_875_876_877_878_879_880_881_882_883_884_885_886_887_888_889_890_891_892_893_894_895_896_897_898_899_900_901_902_903_904_905_906_907_908_909_910_911_912_913_914_915_916_917_918_919_920_921_922_923_924_925_926_927_928_929_930_931_932_933_934_935_936_937_938_939_940_941_942_943_944_945_946_947_948_949_950_951_952_953_954_955_956_957_958_959_960_961_962_963_964_965_966_967_968_969_970_971_972_973_974_975_976_977_978_979_980_981_982_983_984_985_986_987_988_989_990_991_992_993_994_995_996_997_998_999_1000_1001_1002_1003_1004_1005_1006_1007_1008_1009_1010_1011_1012_1013_1014_1015_1016_1017_1018_1019_1020_1021_1022_1023_1024_1025_1026_1027_1028_1029_1030_1031_1032_1033_1034_1035_1036_1037_1038_1039_1040_1041_1042_1043_1044_1045_1046_1047_1048_1049_1050_1051_1052_1053_1054_1055_1056_1057_1058_1059_1060_1061_1062_1063_1064_1065_1066_1067_1068_1069_1070_1071_1072_1073_1074_1075_1076_1077_1078_1079_1080_1081_1082_1083_1084_1085_1086_1087_1088_1089_1090_1091_1092_1093_1094_1095_1096_1097_1098_1099_1100_1101_1102_1103_1104_1105_1106_1107_1108_1109_1110_1111_1112_1113_1114_1115_1116_1117_1118_1119_1120_1121_1122_1123_1124_1125_1126_1127_1128_1129_1130_1131_1132_1133_1134_1135_1136_1137_1138_1139_1140_1141_1142_1143_1144_1145_1146_1147_1148_1149_1150_1151_1152_1153_1154_1155_1156_1157_1158_1159_1160_1161_1162_1163_1164_1165_1166_1167_1168_1169_1170_1171_1172_1173_1174_1175_1176_1177_1178_1179_1180_1181_1182_1183_1184_1185_1186_1187_1188_1189_1190_1191_1192_1193_1194_1195_1196_1197_1198_1199_1200_1201_1202_1203_1204_1205_1206_1207_1208_1209_1210_1211_1212_1213_1214_1215_1216_1217_1218_1219_1220_1221_1222_1223_1224_1225_1226_1227_1228_1229_1230_1231_1232_1233_1234_1235_1236_1237_1238_1239_1240_1241_1242_1243_1244_1245_1246_1247_1248_1249_1250_1251_1252_1253_1254_1255_1256_1257_1258_1259_1260_1261_1262_1263_1264_1265_1266_1267_1268_1269_1270_1271_1272_1273_1274_1275_1276_1277_1278_1279_1280_1281_1282_1283_1284_1285_1286_1287_1288_1289_1290_1291_1292_1293_1`

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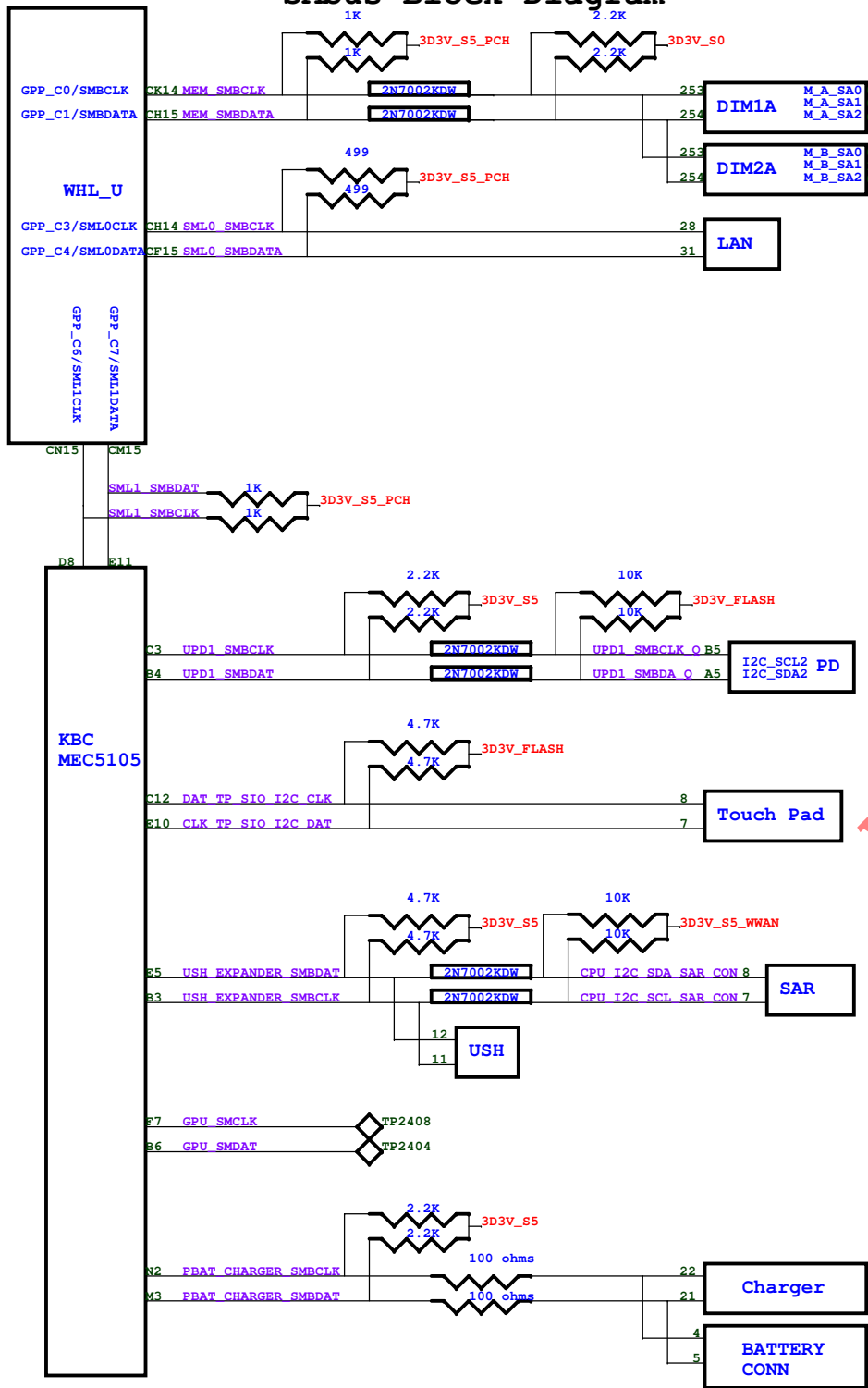




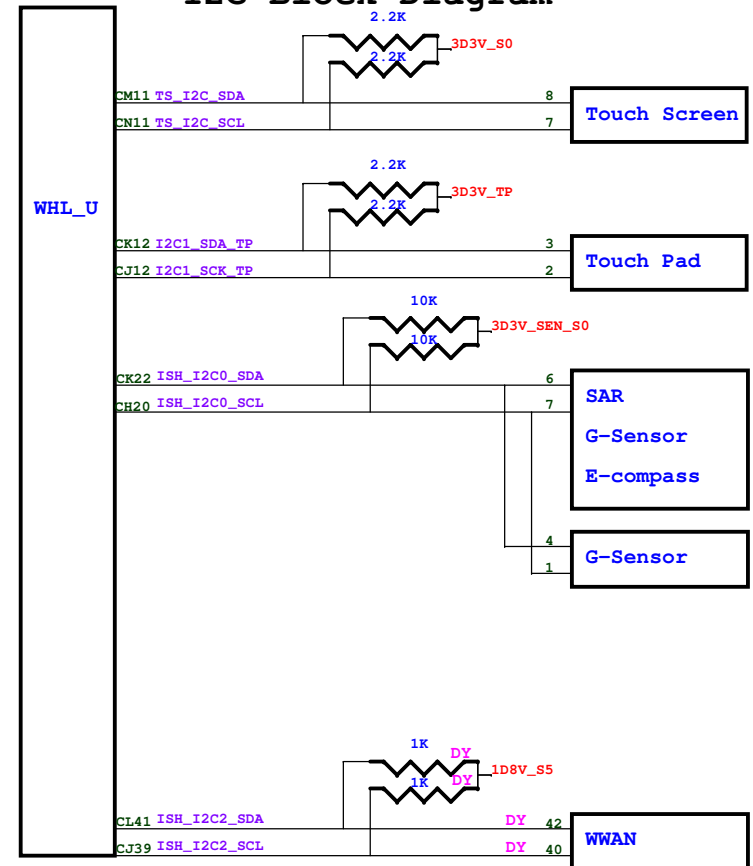
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Title			Power Block Diagram	
Size	Document Number	Bandon / NorthBay 13"		Rev
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## SMbus Block Diagram



## I2C Block Diagram



## LAN DATASHEET

Pin Name	Pin #	Type	Op Mode	Name and Function
SMB_CLK	28	O/d	Bi-dir	SMBus clock. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499k resistor (while in Sx mode).
SMB_DATA	31	O/d	Bi-dir	SMBus data. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499k resistor (while in Sx mode).

**Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship**

Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance ( $C_b$ )	External Pull-up	PCH Pull Down Strength (Refer EDS)
Upto 400 pF	2.2K $\Omega$	100 $\Omega$
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings		
Total Bus Capacitance ( $C_b$ )	External Pull-up	PCH Pull Down Strength

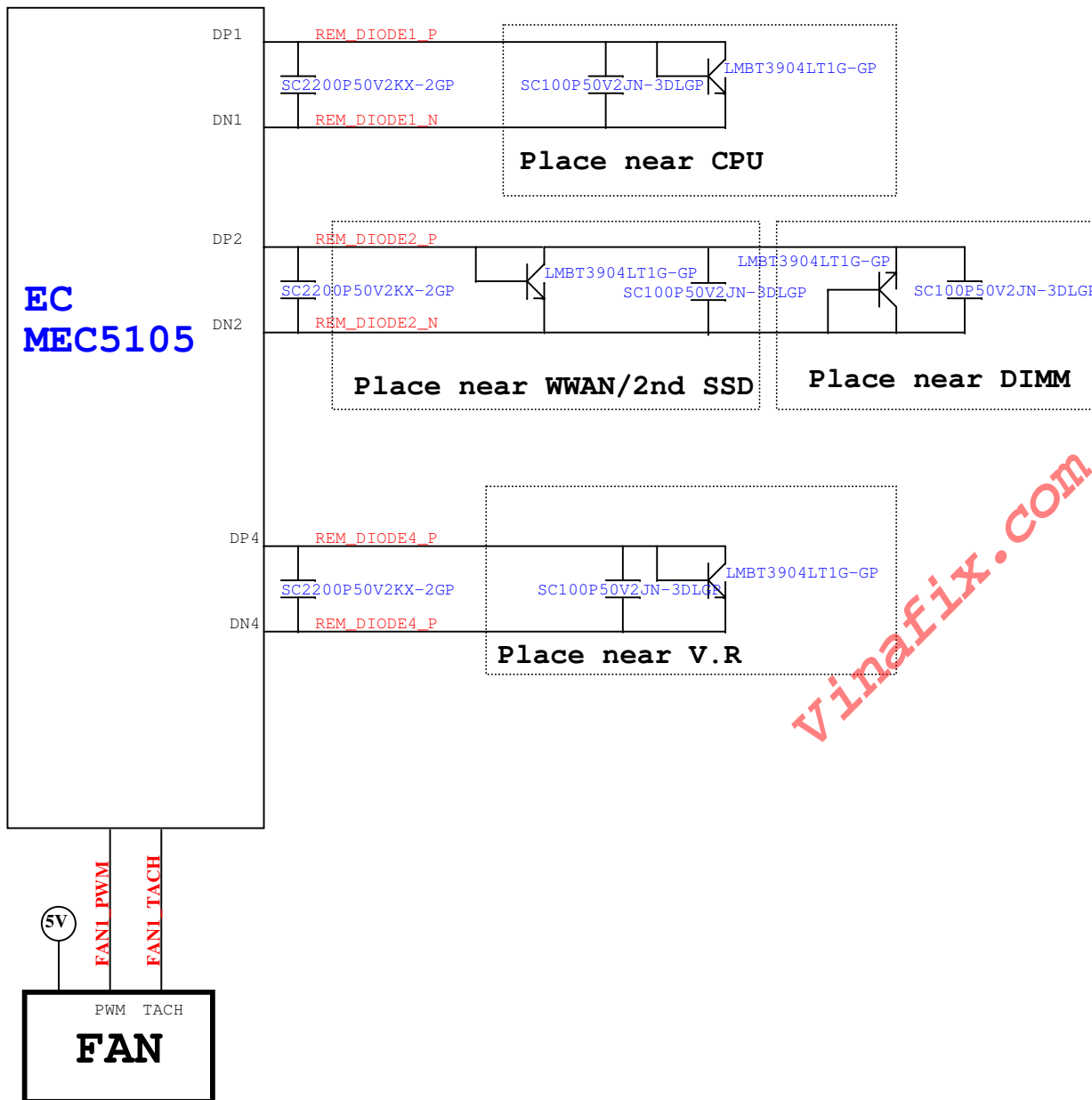
Upto 100pF	2.7KΩ	100Ω
Upto 200pF	1.5KΩ	
Upto 300pF	1KΩ	
Upto 400 pF	680Ω	
<b>Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings</b>		
<b>Total Bus Capacitance (C<sub>b</sub>)</b>	<b>External Pull-up</b>	<b>PCH Pull Down Strength</b>
Upto 50pF	2.2KΩ	100Ω
Upto 100pF	1.2KΩ	
Upto 200pF	560Ω	
Upto 300pF	390Ω	
Upto 400 pF	270Ω	67Ω

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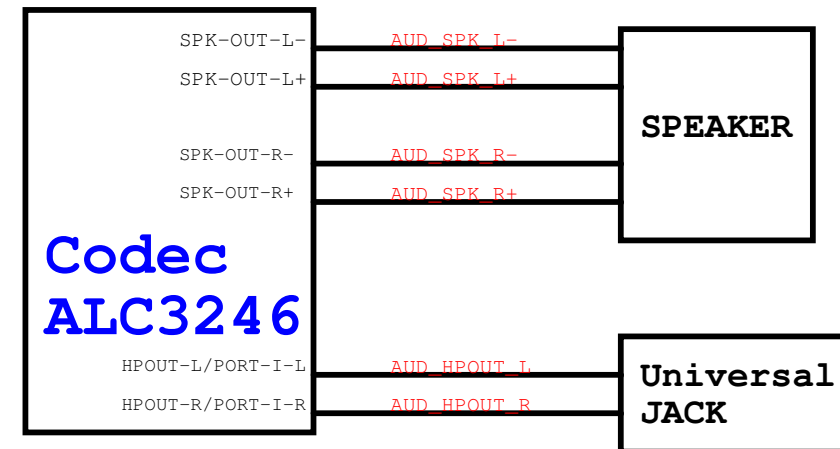




# Thermal Block Diagram



# Audio Block Diagram



<Core Design>



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Title **THERMAL/AUDIO BLOCK DIAGRAM**

Size A4 Document Number **Bandon / NorthBay 13"** Rev **X00**

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Title <b>CLK Block</b>			
Size A4	Document Number <b>Bandon / NorthBay 13"</b>		Rev <b>X00</b>
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